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PWB: XXXXX
DATE: 1450-06

ZZZ1



PCB 305 LA-K472P REV0 MB 17" S
DAB00075000
PCB@

Dell/Compal Confidential

Schematic Document

(Horizon Tiger Lake H with nVIDIA GN20)

DVT2

2021-02-18

Rev: 0.3 (X02)

BOM Structure

PCB@ : PCB PN
PCH@: PCH P/N
EC@: EC Chip P/N
NV@: BIOS board ID (GPU type)
N18EG0@/N18EG1@/N18EG2@/N18EG3@/N18EG1B@: GPU_ID & GPU Chip
TYPEC@/RTD3@: TBT
G0G1G3Q@/G1G2@/G3P@: OVR(NV)
NG3P@: OVRM(ARD request)
CMC@: CMC Debug Port
RF@/EMI@/ESD@/ TYPEC@RF@ : EMI, ESD and RF Component
CONN@:Connector

@TBT@:TBT RTD3 Un-POP Component
MCNGD8A@/MCNGD6A@/SAMGD6A@/SAMGD8A@:VRAM CHIP
VRAM_S@/VRAM_M@: VRAM strap pin
@: Un-pop Component

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				Date	Thursday, February 18, 2021
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				Rev	0.3

Board ID Table for AD channel

Vcc		3.1V +/- 1%			
Ra		100K +/- 1%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.000V	0x00 - 0x17
1	12K +/- 1%	0.323V	0.332V	0.342V	0x18 - 0x1E
2	15K +/- 1%	0.393V	0.404V	0.416V	0x1F - 0x25
3	20K +/- 1%	0.503V	0.517V	0.531V	0x26 - 0x30
4	27K +/- 1%	0.642V	0.659V	0.676V	0x31 - 0x3A
5	33K +/- 1%	0.750V	0.769V	0.789V	0x3B - 0x45
6	43K +/- 1%	0.910V	0.932V	0.955V	0x46 - 0x53
7	56K +/- 1%	1.088V	1.112V	1.138V	0x54 - 0x64
8	75K +/- 1%	1.300V	1.329V	1.357V	0x65 - 0x76
9	100K +/- 1%	1.519V	1.550V	1.581V	0x77 - 0x88
10	130K +/- 1%	1.720V	1.752V	1.785V	0x89 - 0x96
11	160K +/- 1%	1.874V	1.908V	1.941V	0x97 - 0xA3
12	200K +/- 1%	2.032V	2.067V	2.101V	0xA4 - 0xAF
13	240K +/- 1%	2.153V	2.188V	2.223V	0xB0 - 0xB7
14	270K +/- 1%	2.227V	2.262V	2.297V	0xB8 - 0xBF
15	330K +/- 1%	2.344V	2.37V	2.413V	0xC0 - 0xC9
16	430K +/- 1%	2.480V	2.515V	2.550V	0xCA - 0xD4
17	560K +/- 1%	2.596V	2.630V	2.665V	0xD5 - 0xDD
18	750K +/- 1%	2.701V	2.735V	2.769V	0xDE - 0xE6
19	1.2M +/- 1%	2.829V	2.862V	2.895V	0xE7 - 0xFF

PCIE CLK table

PCIE CLK	PCB Revision
0	GPU
1	
2	
3	SSD1
4	SSD2
5	LAN
6	
7	WLAN

Board ID table

NV	PCB Revision (GDS70)
GN20	
2	EVT-1
6	DVT-1
10	DVT-2
14	Pilot

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_DDR	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VALW	+1.8VALW power rail for PCH	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF				

PCH-H HM570

HSIO	USB3.1	PCIe	SATA3	Function
0	1			Type-A(IO/B)
1	2			Type-C
2	3			Type-A(IO/B)
3	4			Card reader(IO/B)
4	5			N/A
5	6			N/A
6	7	1		N/A
7	8	2		N/A
8	9	3		N/A
9	10	4		N/A
10		5		LAN
11		6		SIP WLAN
12		7		N/A
13		8		N/A
14		DMI8		N/A
15		DMI7		N/A
16		DMI6		N/A
17		DMI5		N/A
18		DMI4		CPU to PCH
19		DMI3		
20		DMI2		
21		DMI1		
22		9		N/A
23		10		N/A
24		11	0a	N/A
25		12	1a	N/A
26		13	0b	N/A
27		14	1b	N/A
28		15	2	N/A
29		16	3	N/A
30		17	4	N/A
31		18	5	N/A
32		19		N/A
33		20		N/A
34		21		N/A
35		22		N/A
36		23		N/A
37		24		N/A

USB2	Function
1	TBT Type-C
2	Type-C
3	Type-A(IO/B)
4	ELC
5	Card reader(IO/B)
6	Type-A(IO/B)
7	Camera
8	N/A
9	Per Key(MCU/B)
10	N/A
11	N/A
12	N/A
13	N/A
14	WLAN+BT

Symbol Note :

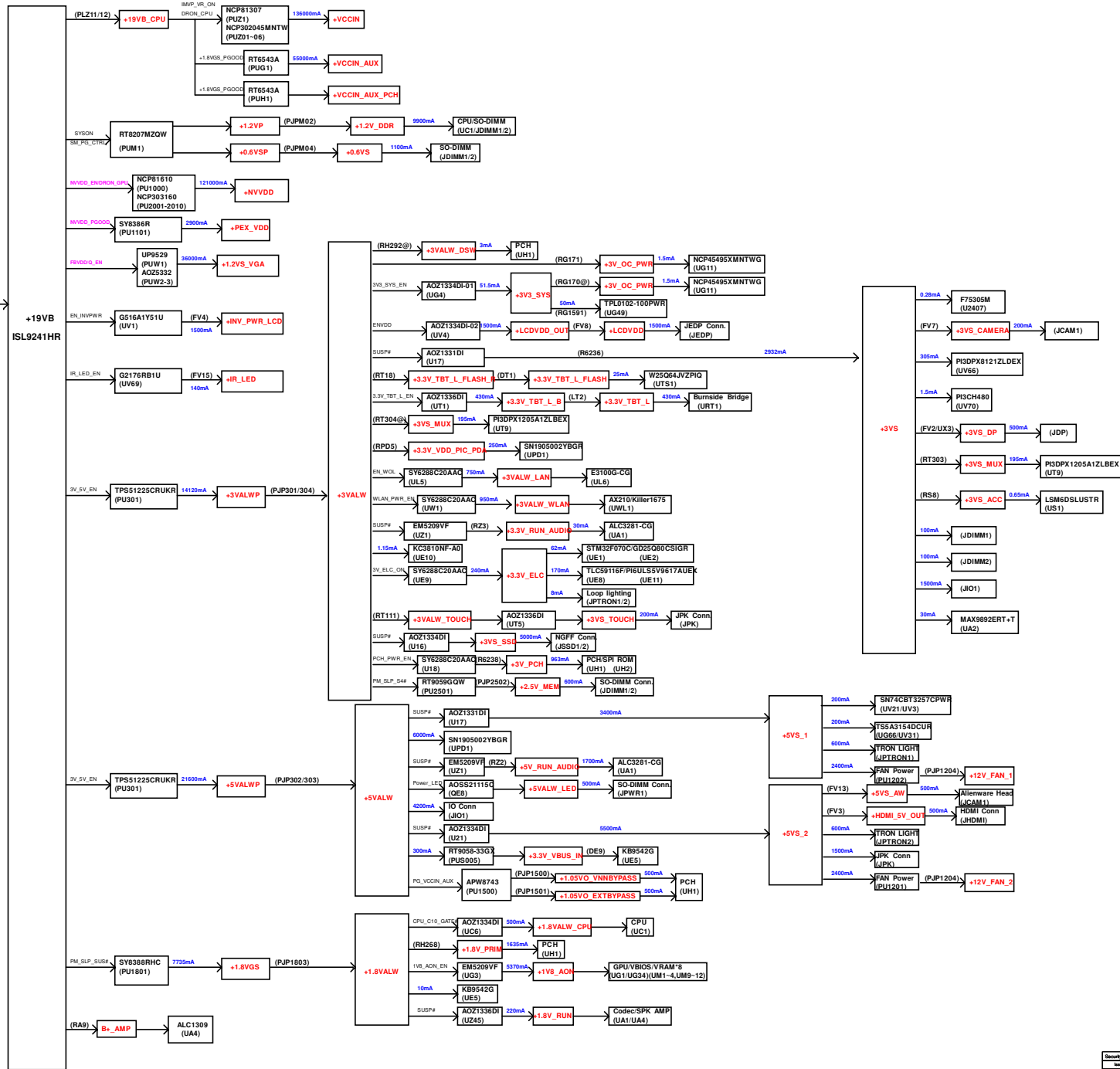


Digital Ground



Analog Ground

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01/27 DVT2 Modify

UC1



FH8069004351613 QXJ1 R0 2.7G S
SA0000EDJOL
QXJ1@

UC1



FH8069004352018 QXHY R0 2.3G S
SA0000EDKOL
QXHY@

UC1

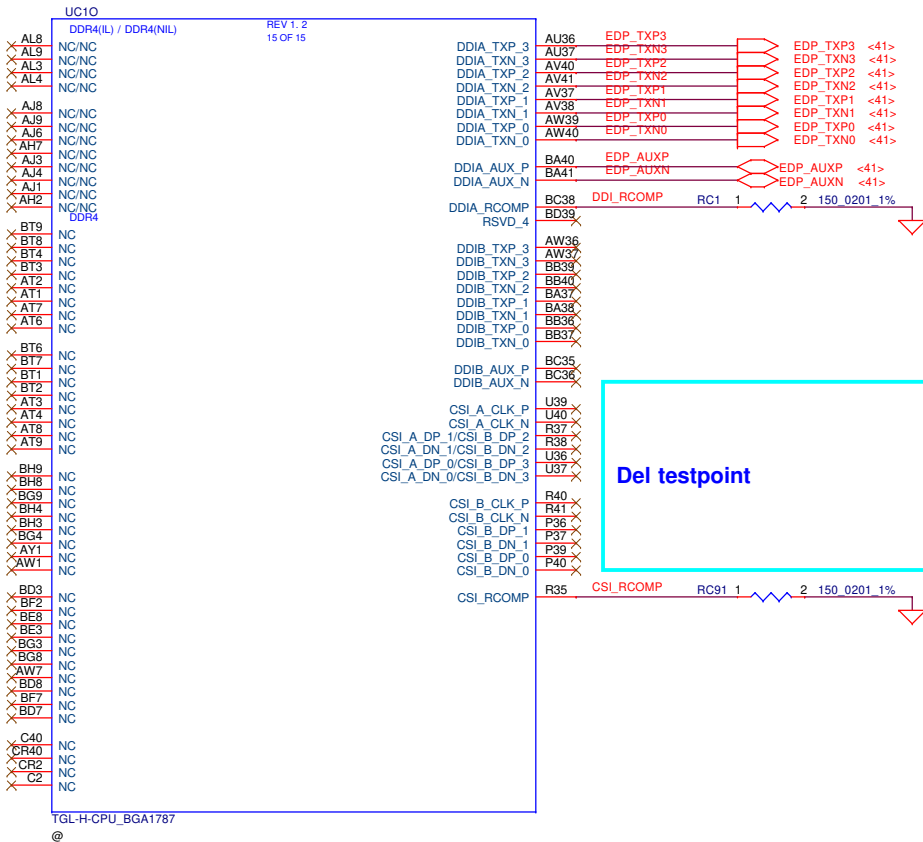


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QXD0@

UC1

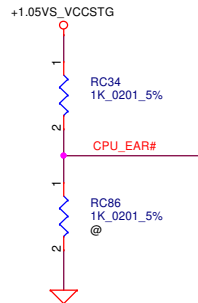


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QXCW@

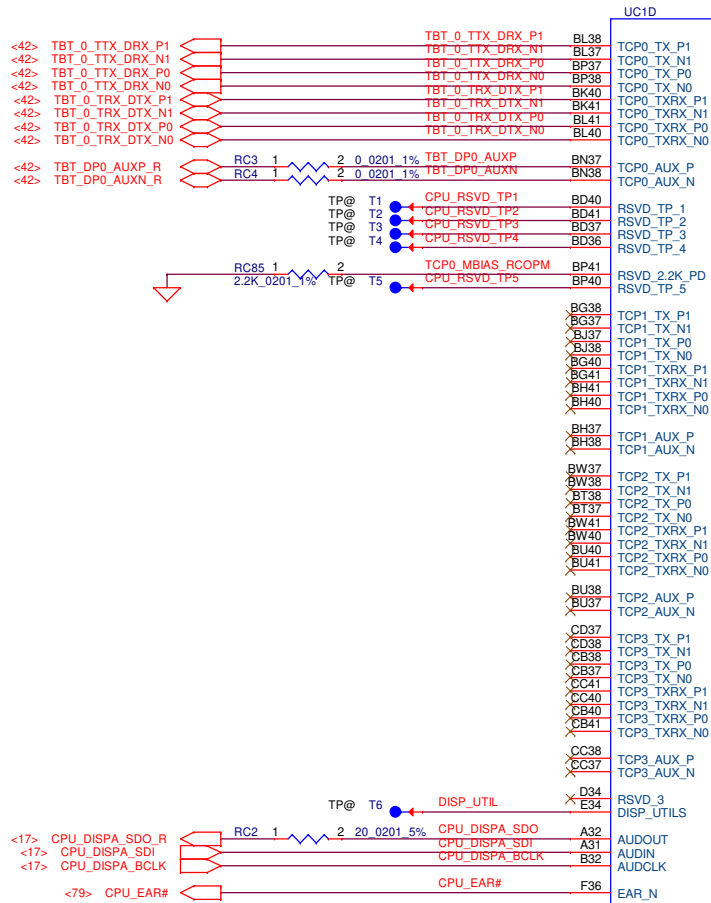


eDP

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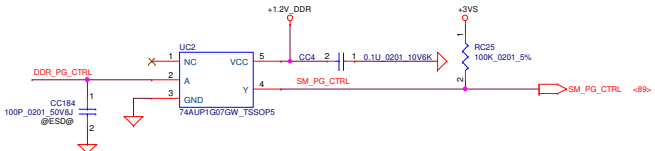
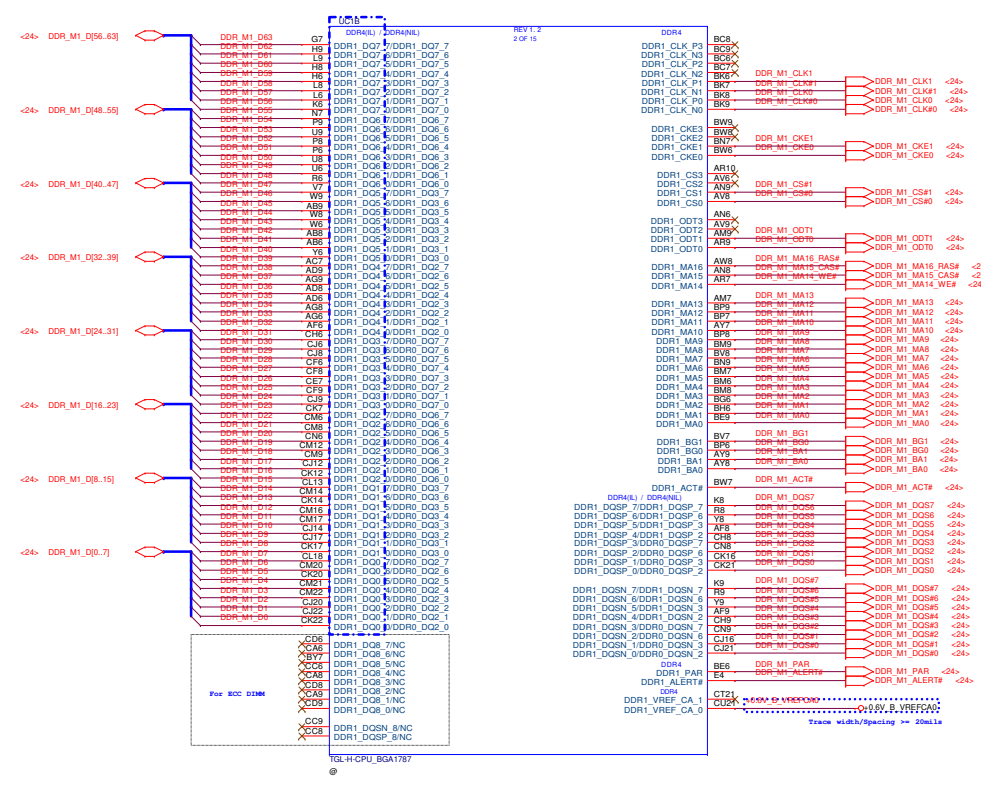


EAR#
 Stall CPU reset sequence until de-asserted:
 1 = (Default) Normal Operation No stall.
 0 = Stall

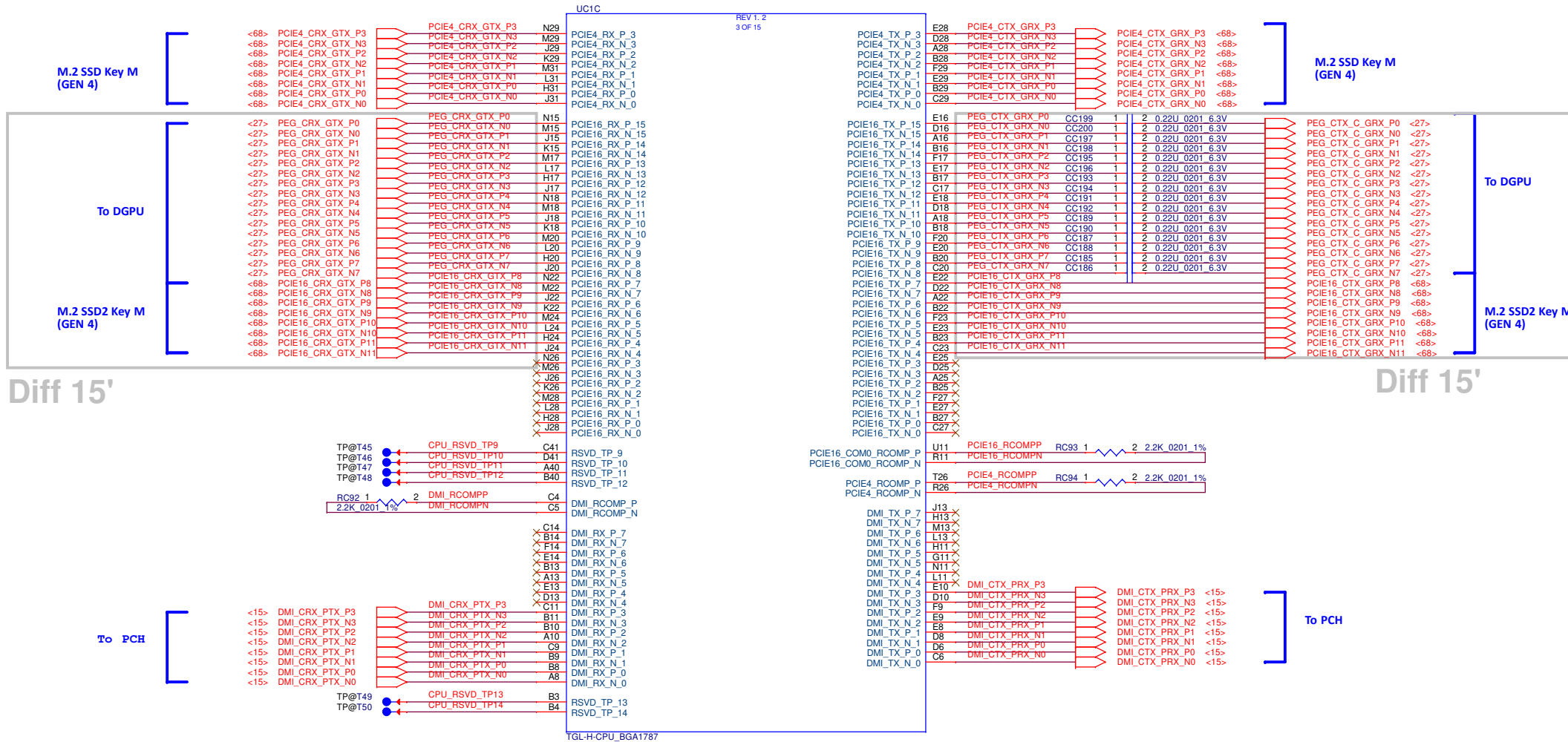


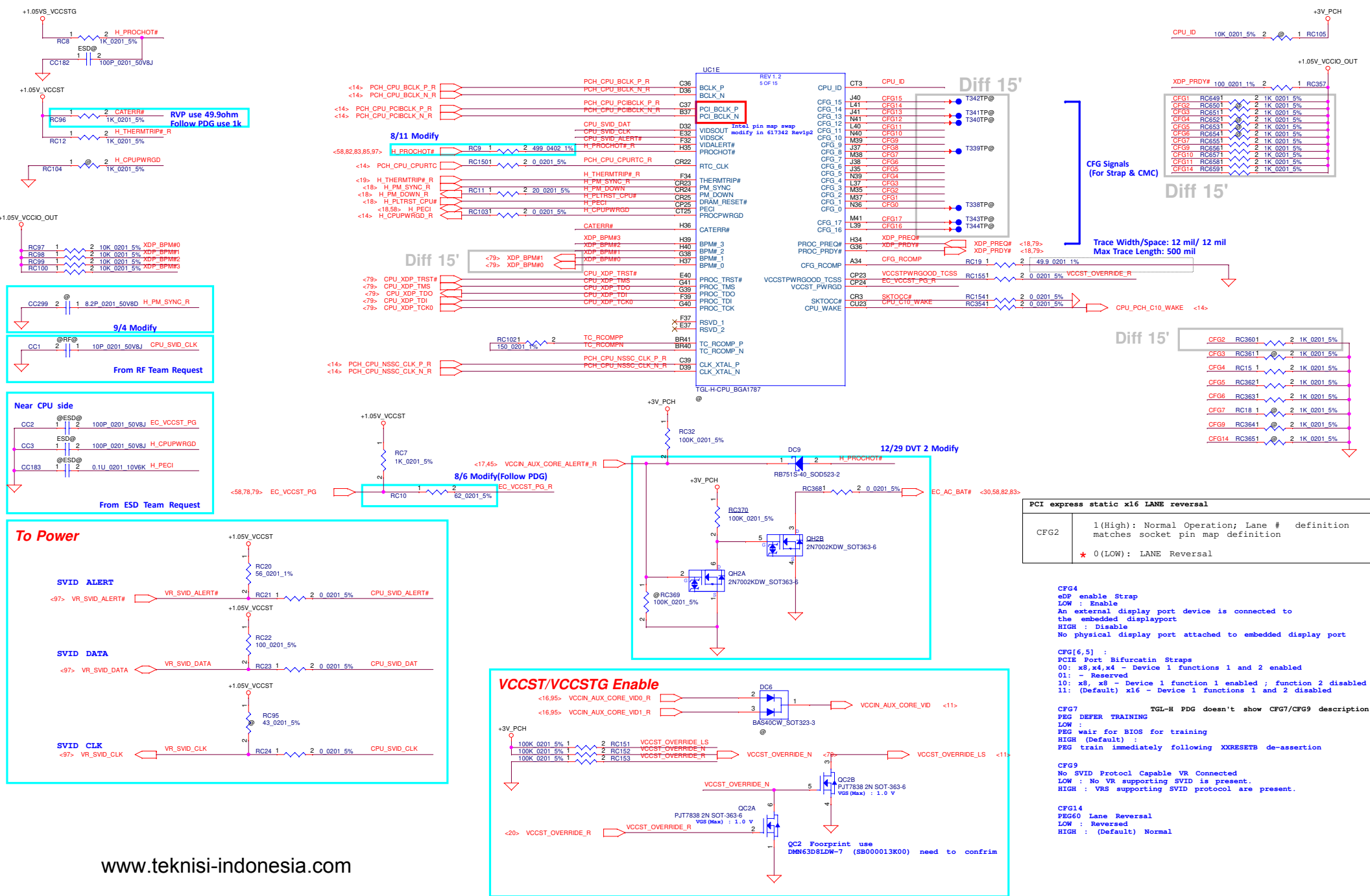
TGL-H-CPU_BGA1787
 @

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						Size		Document Number		Rev	
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Issued Date	2020/04/10	Deciphered Date	2021/12/31		
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PCI express static x16 LANE reversal	
CFG2	1(High): Normal Operation; Lane # definition matches socket pin map definition ★ 0(LOW): LANE Reversal

CFG4
xDP enable Strap
LOW : Enable
An external display port device is connected to the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port

CFG[6,5] :
PCIe Port Bifurcation Straps
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
01: - Reserved
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
11: (Default) x16 - Device 1 functions 1 and 2 disabled

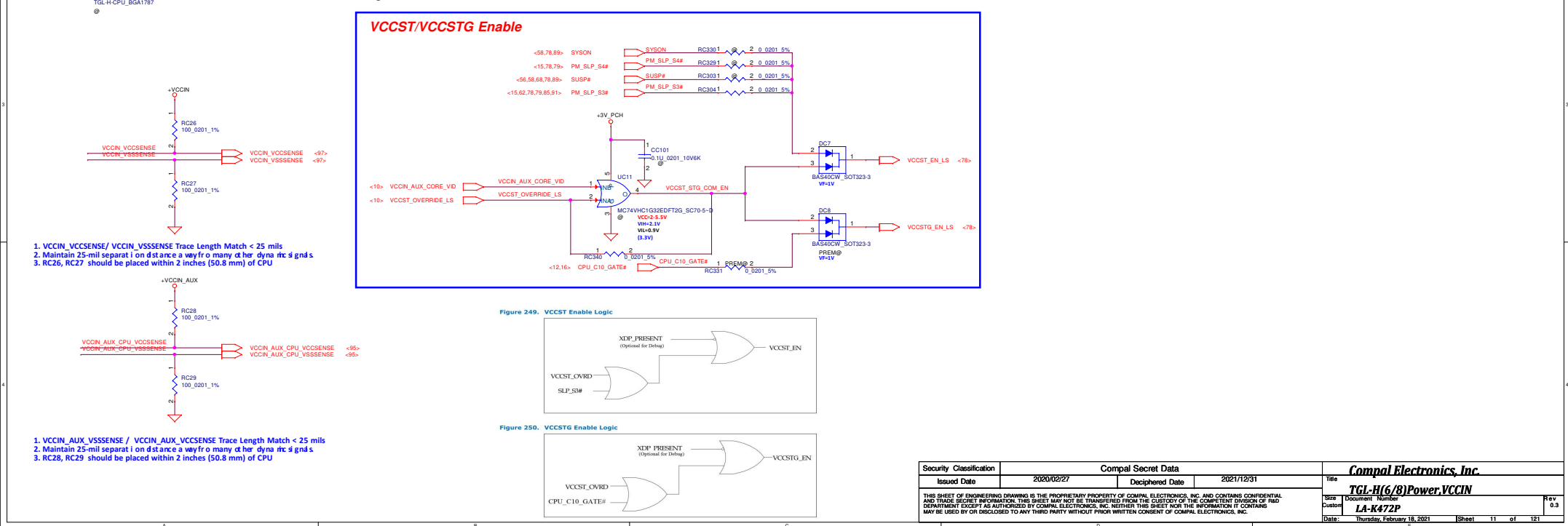
CFG7
TGL-H PDG doesn't show CFG7/CFG9 description
PEG DEFER TRAINING
LOW :
PEG wait for BIOS for training
HIGH (Default) :
PEG train immediately following XKRESETB de-assertion

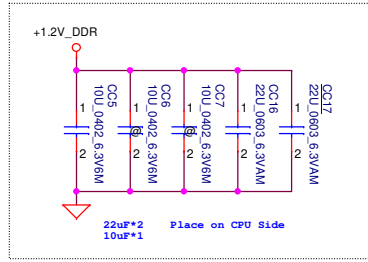
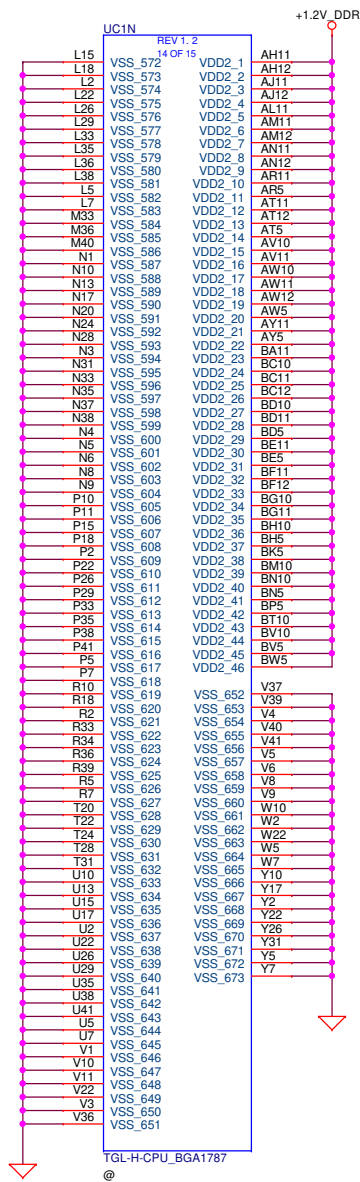
CFG9
No SVID Protocol Capable VR Connected
LOW : No VR supporting SVID is present.
HIGH : VRS supporting SVID protocol are present.

CFG14
PEG60 Lane Reversal
LOW : Reversed
HIGH : (Default) Normal

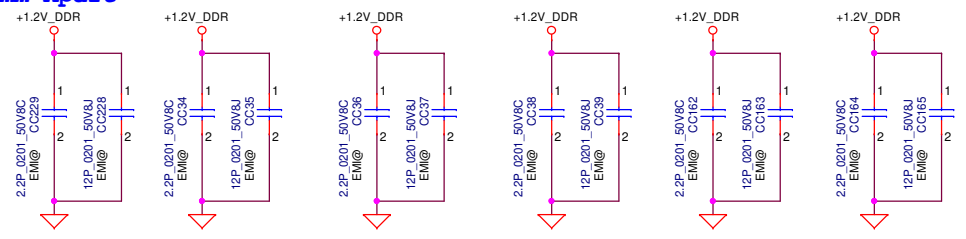
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Issued Date	2020/02/27	Deciphered Date	2021/12/31	Document Number	TGL-H(5/8)CFG/Sideband
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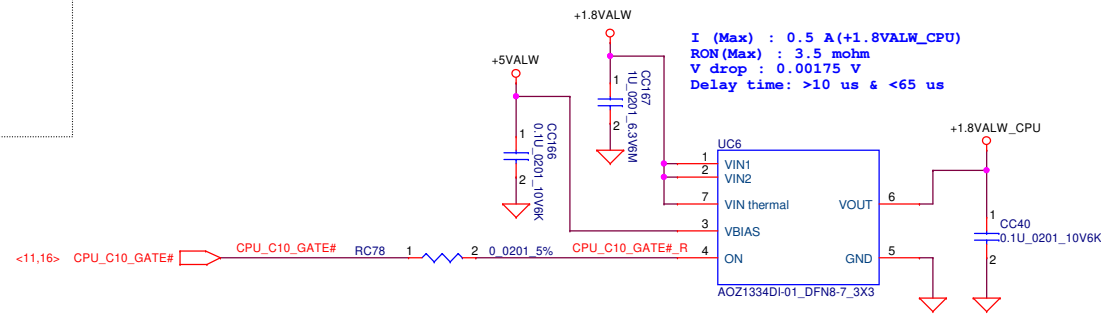
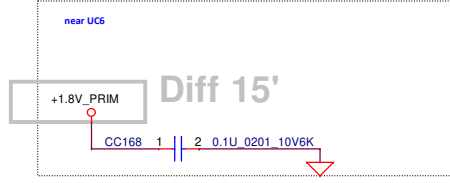




EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 6 (EMI@)
2.2pF* 6 (EMI@)

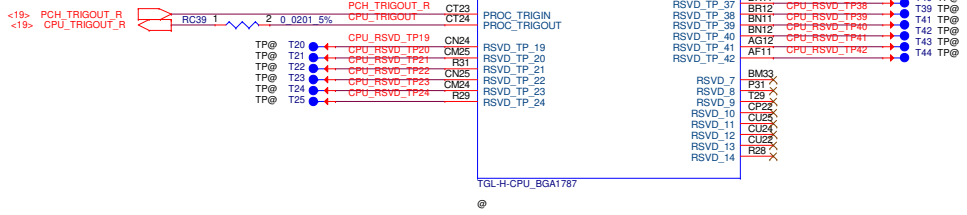
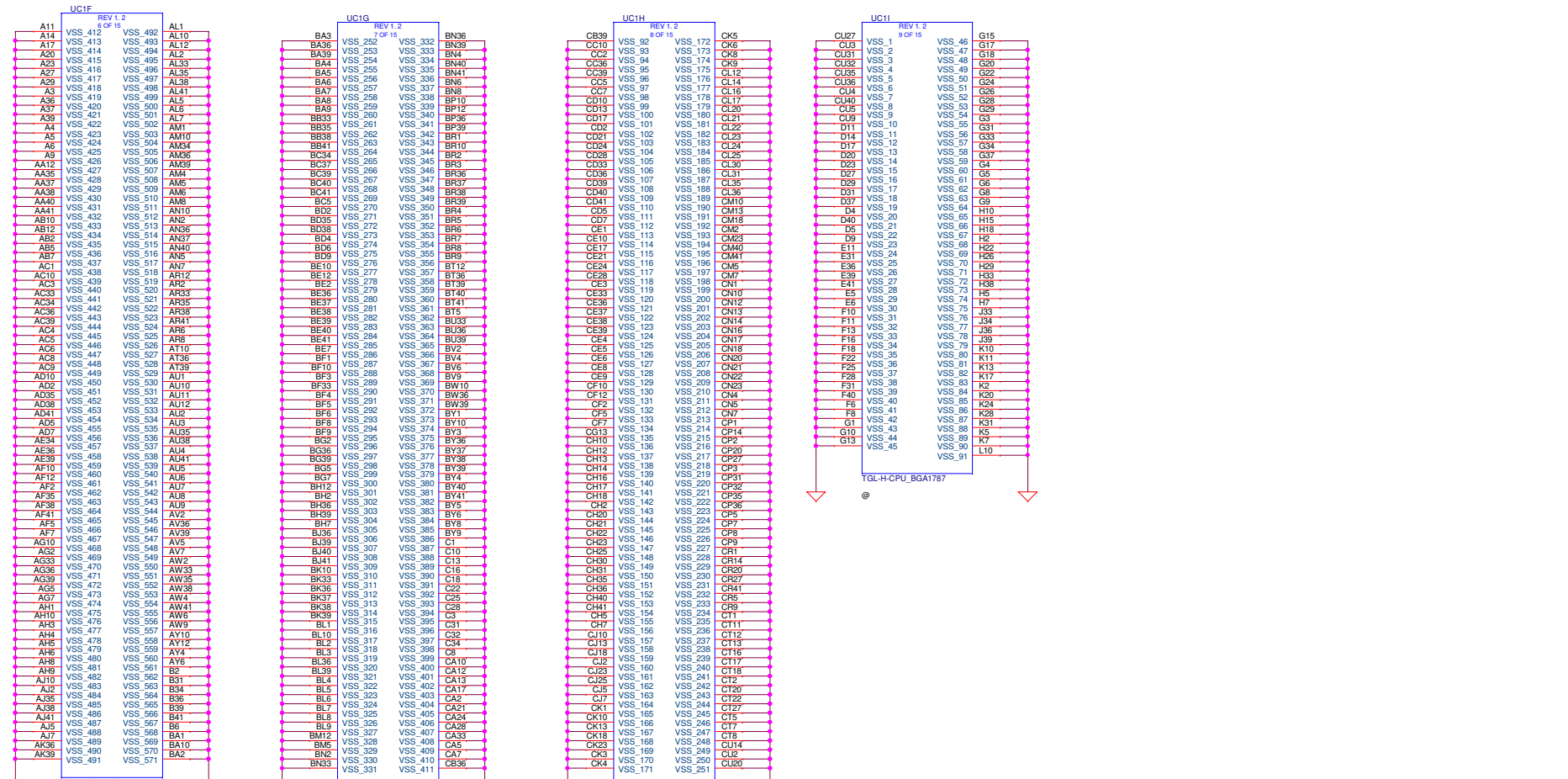


RVP doesn't have PU.
Follow TD team and change Power rail



I (Max) : 0.5 A(+1.8VALW_CPU)
RON(Max) : 3.5 mohm
V drop : 0.00175 V
Delay time : >10 us & <65 us

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FH82HM570 QWC2 B0 FCBGA PCH-H S
SA0000EDM0L
PCH@

12/29 DVT2 Modify(reserve for CLK PN swap)

@ RH1710 1 2 0 0201 5%
@ RH1711 1 2 0 0201 5%

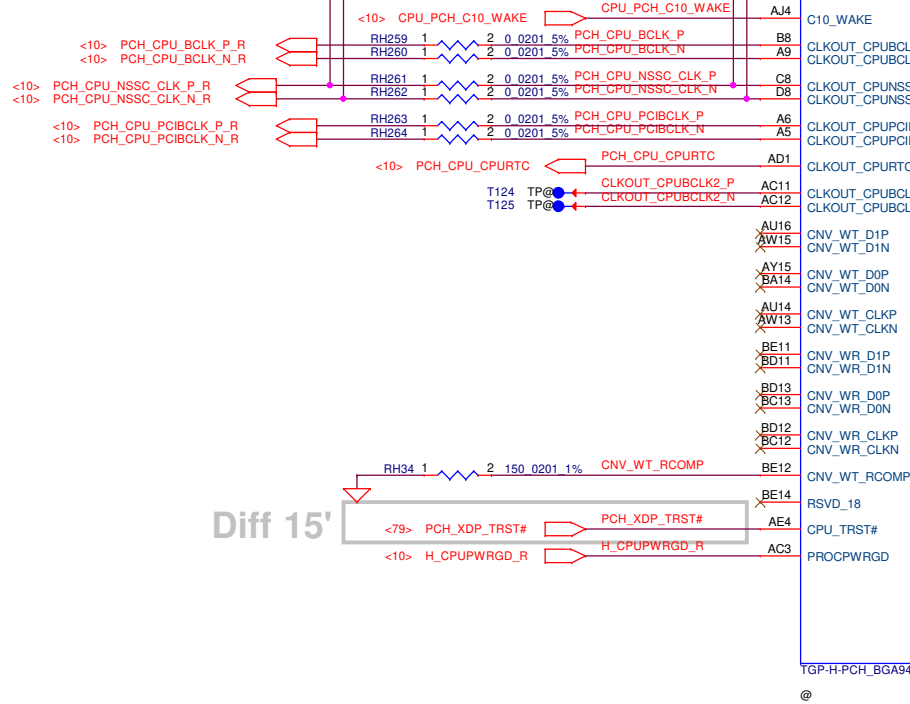
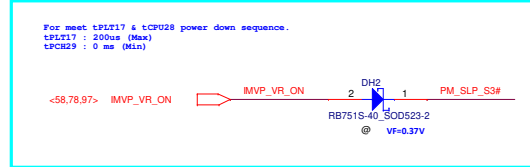
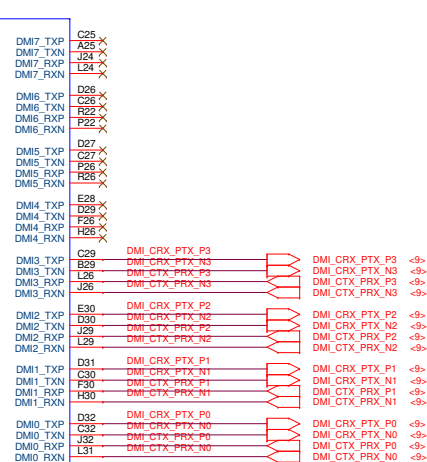
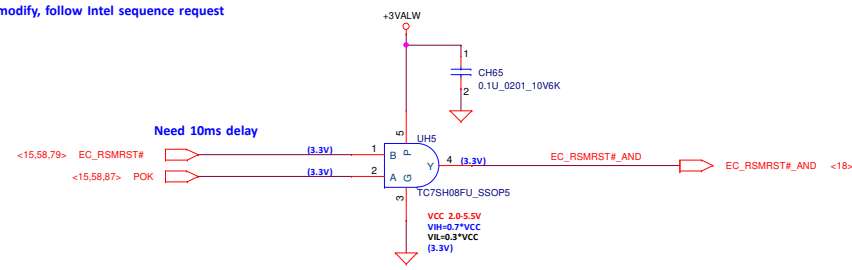
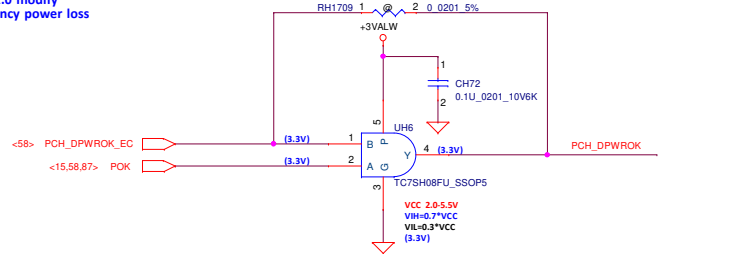
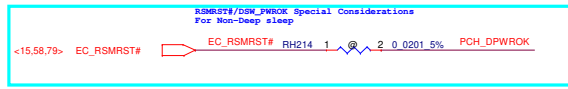
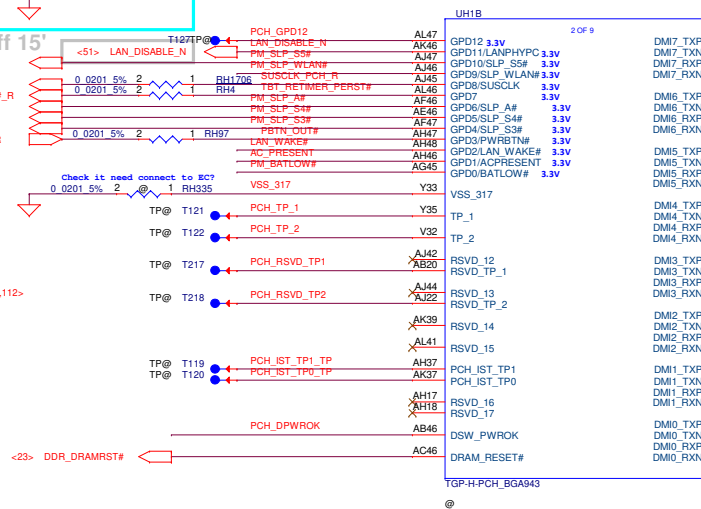
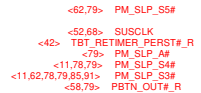
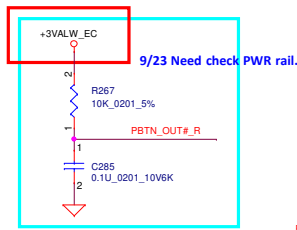


Table 65. Platform Clocks and Associated Signal Details and Descriptions

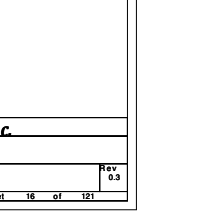
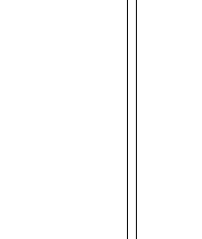
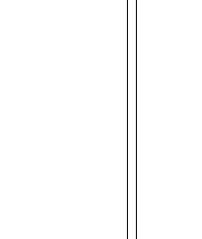
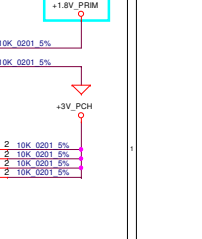
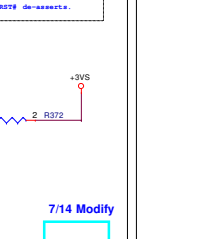
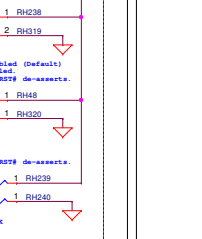
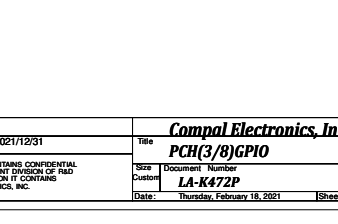
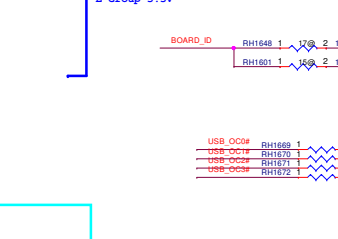
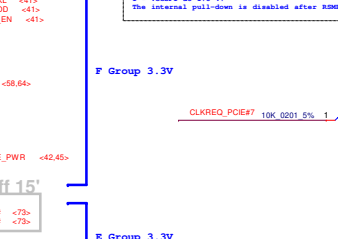
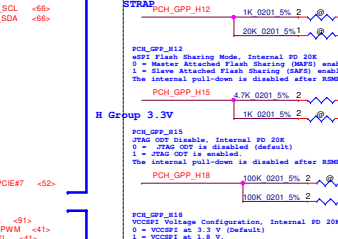
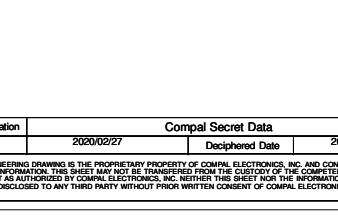
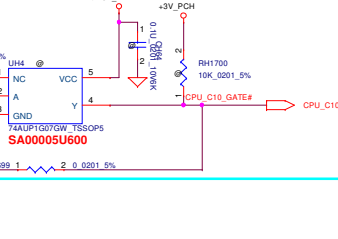
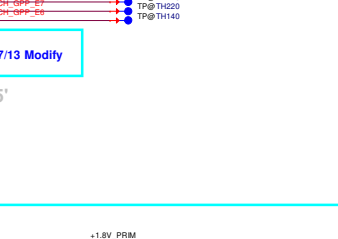
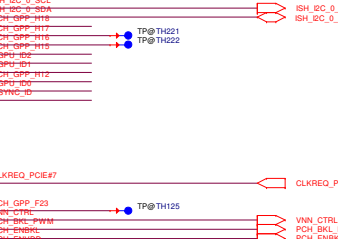
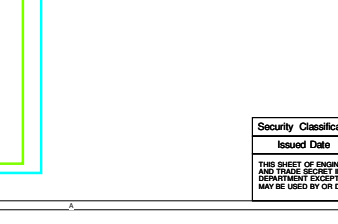
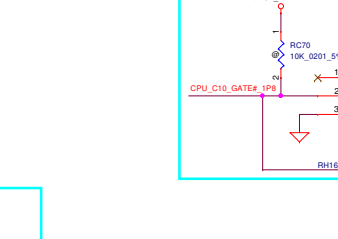
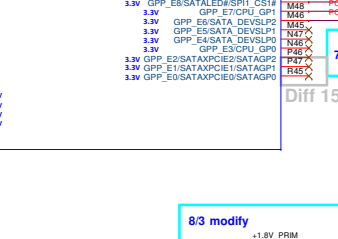
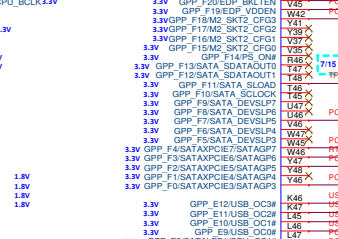
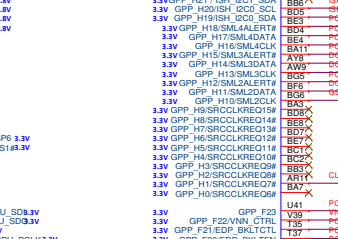
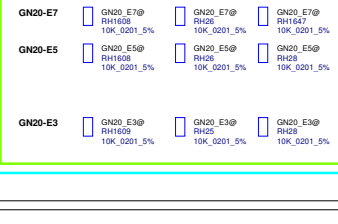
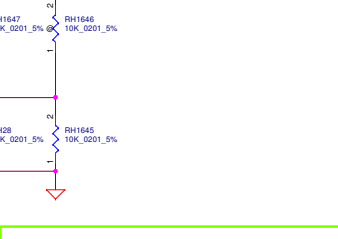
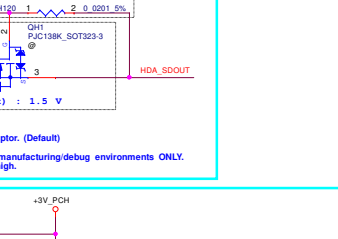
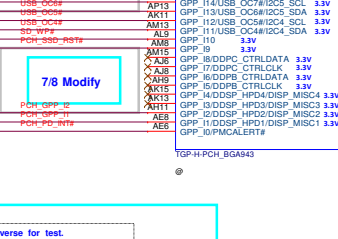
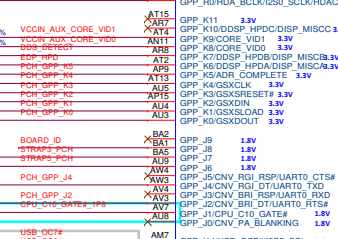
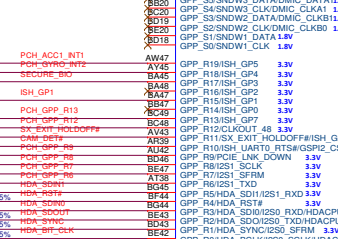
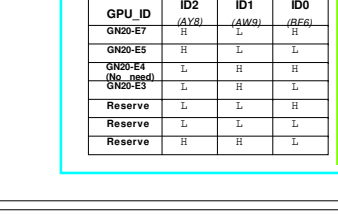
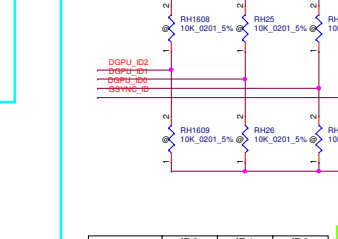
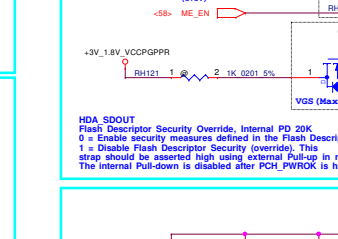
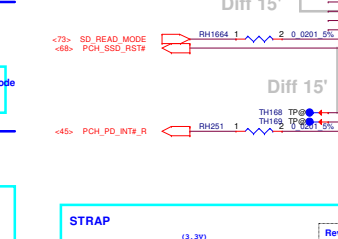
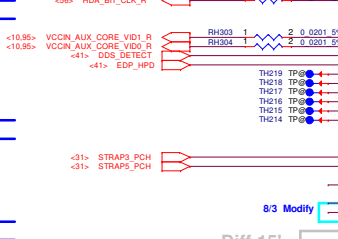
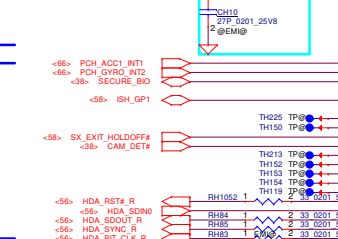
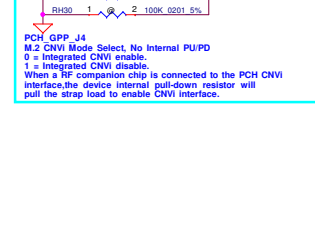
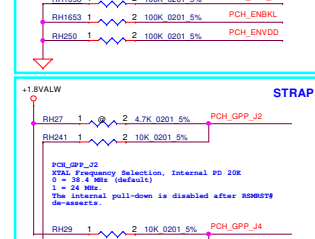
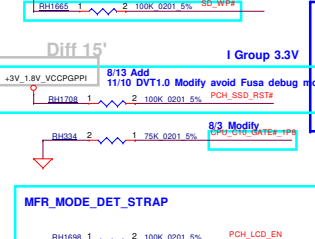
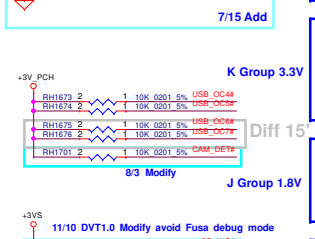
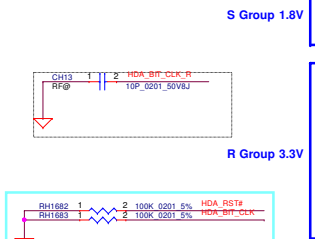
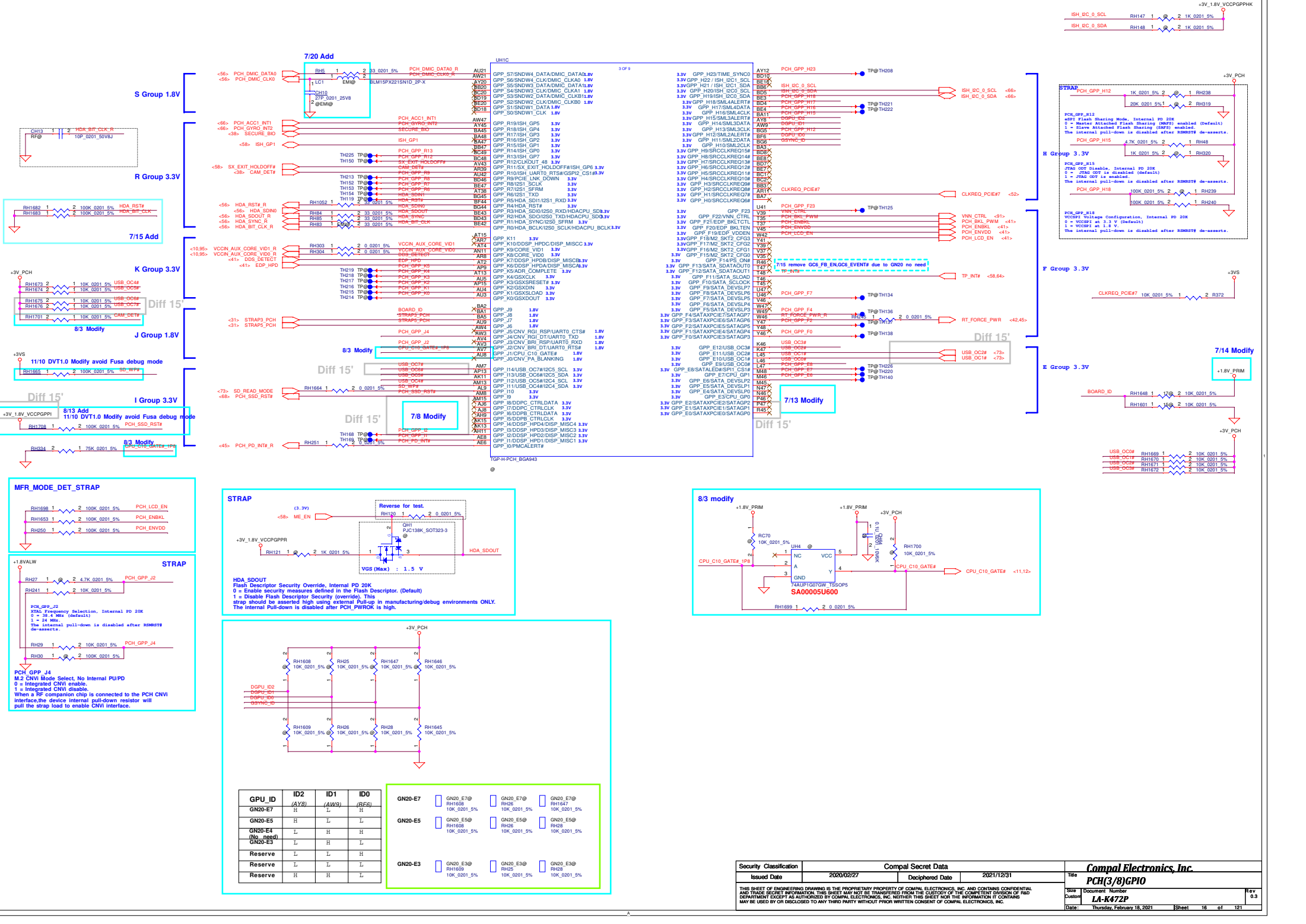
Signal Name	Type	SSC Capable	Description
CLKOUT_CPUNSSC_P CLKOUT_CPUNSSC_N	O	No	Filtered Crystal Reference Clock to CPU: 24MHz differential, filtered crystal reference clock to the processor
CLKOUT_CPUBCLK_P CLKOUT_CPUBCLK_N	O	Yes	Differential Clock to CPU: Reference clock to the processor 100-MHz differential core
CLKOUT_CPUPCIBCLK_P CLKOUT_CPUPCIBCLK_N	O	Yes	Differential PCIe* Reference Clock to CPU: 100-MHz PCIe* 3.0 specification compliant differential PCIe* reference clock to the processor
CLKOUT_PCIE_P[15:0] CLKOUT_PCIE_N[15:0]	O	Yes	PCI Express* Clock Output: PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices. <ul style="list-style-type: none">CLKOUT_PCIE_P/N [15:0] = Can be used for PCIe* Gen1/2/3 supportCLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support

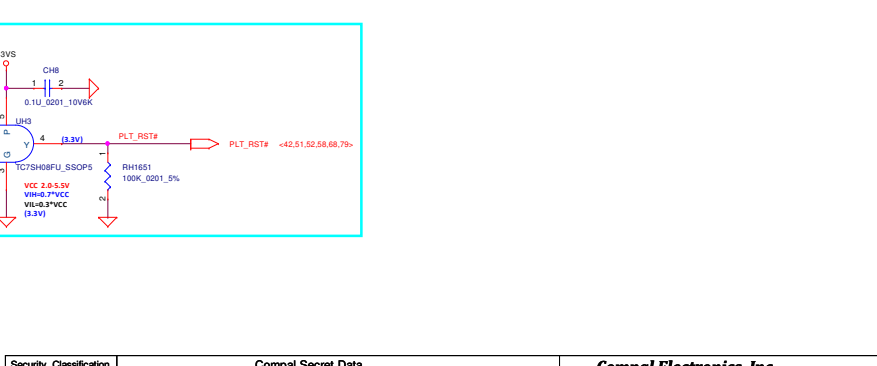
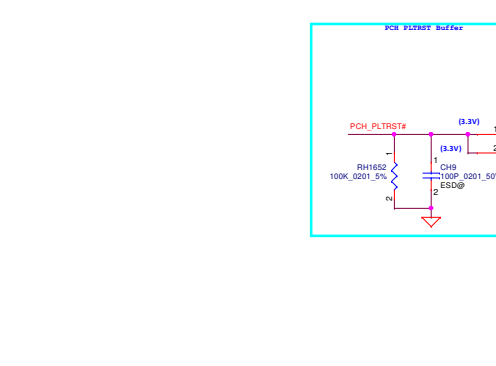
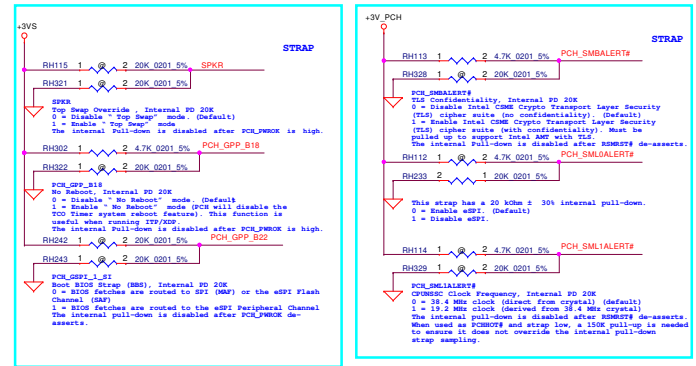
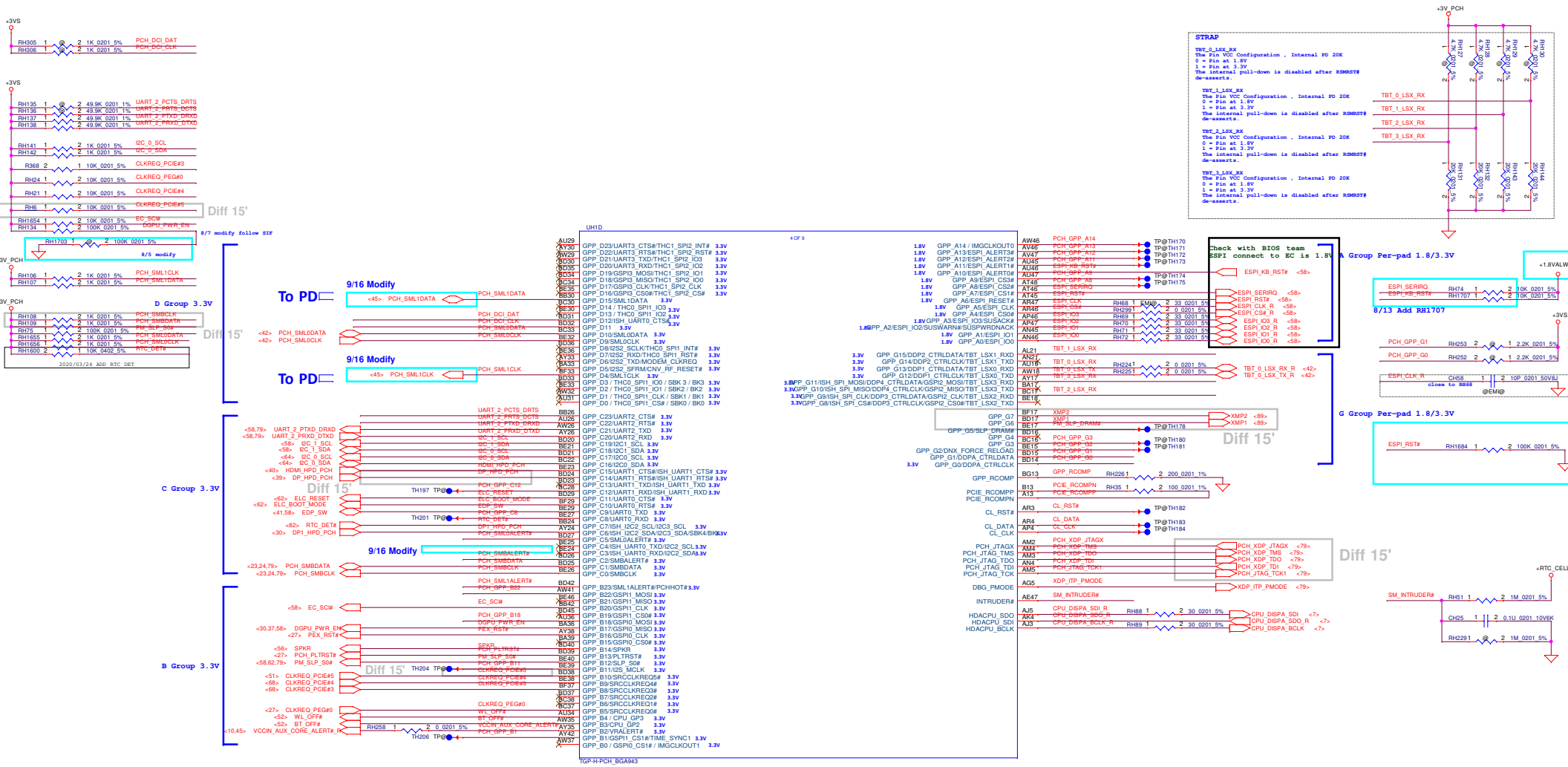
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						Size		Document Number		Rev	
						Custom		LA-K472P		0.3	
						Date:		Thursday, February 18, 2021		Sheet 14 of 121	

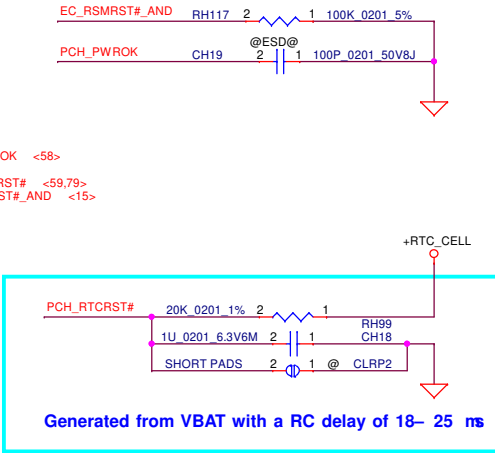
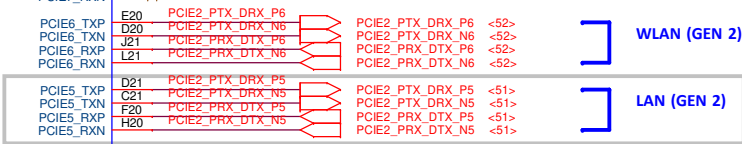
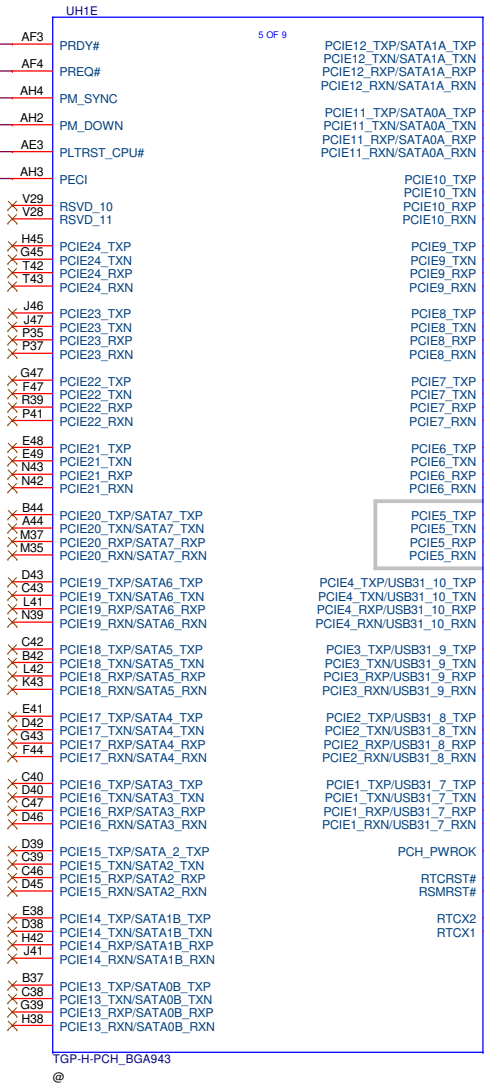
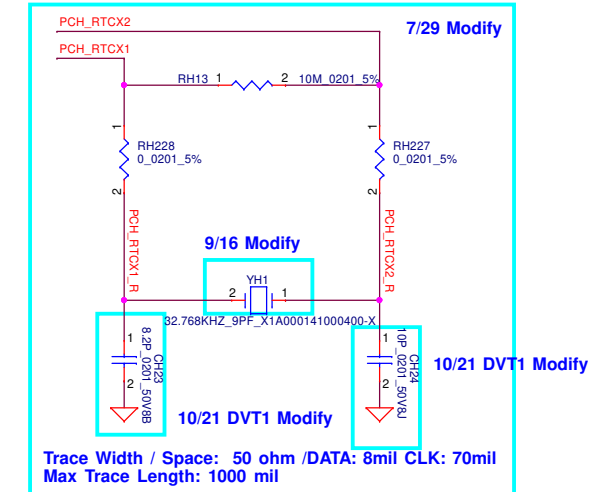
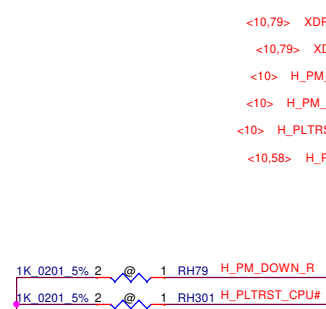


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				Date:	Thursday, February 18, 2021	Sheet 15 of 121

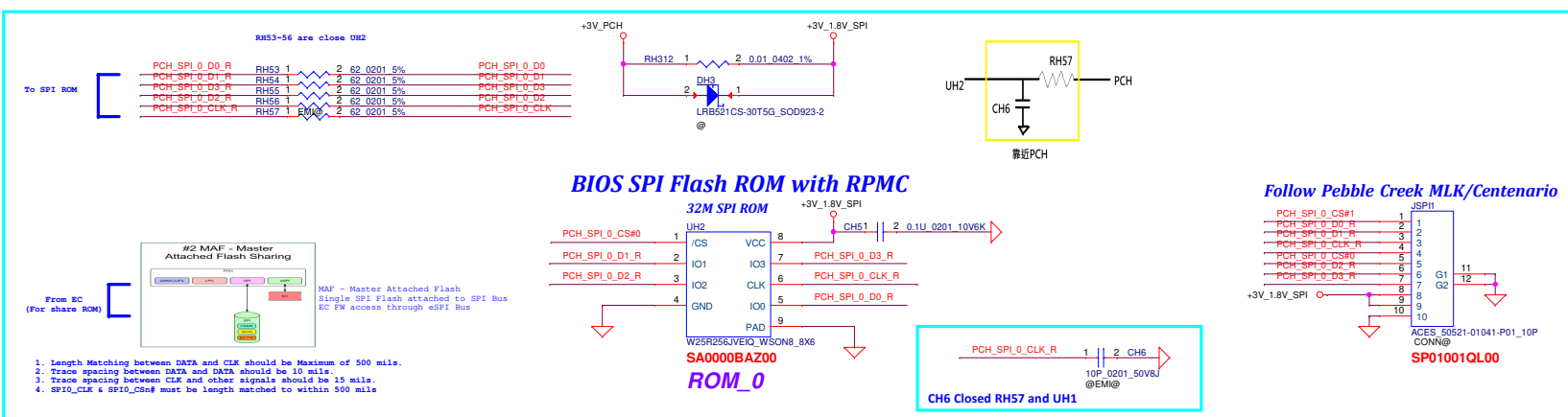
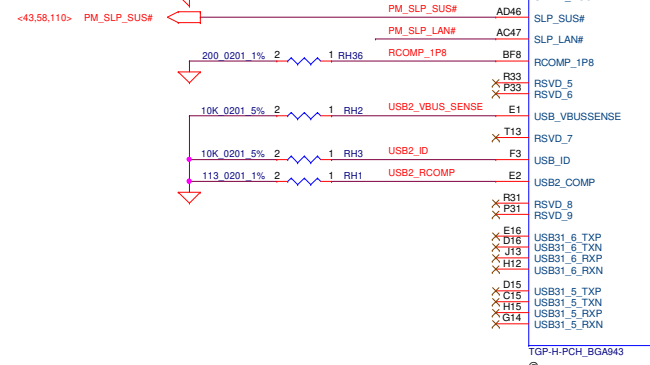
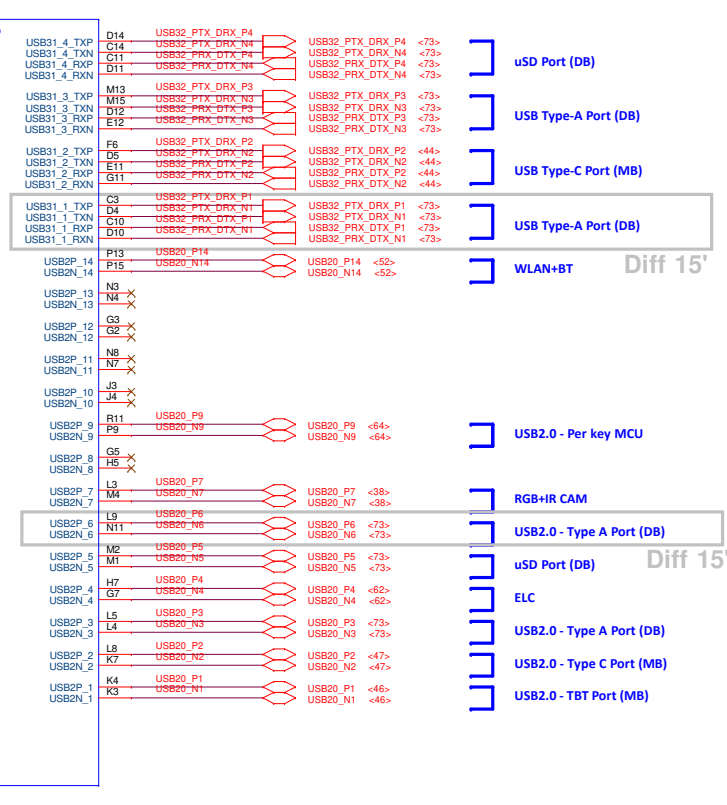




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Size		Document Number			
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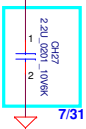


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GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPRIM_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V (Per-pad voltage configuration)
Primary Well Group B (GPP_B) Primary Well Group C (GPP_C)	VCCPGPBC	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group D (GPP_D)	VCCPGPDD	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group E (GPP_E) Primary Well Group F (GPP_F)	VCCPGPEF	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group G (GPP_G)	VCCPGGP_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V (Per-pad voltage configuration)
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPHK	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group I (GPP_I)	VCCPGPI	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8 V Only
Primary Well Group R (GPP_R)	VCCPGPPR	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group S (GPP_S)	VCCPRIM_1P8	1.8 V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only



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UH1H		
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A17	VSS_163	AJ23
A2	VSS_164	AJ25
A28	VSS_165	AJ27
A3	VSS_166	AJ28
A33	VSS_167	AK12
A37	VSS_168	AK17
A4	VSS_169	AK18
A41	VSS_170	AK24
A45	VSS_171	AK25
A46	VSS_172	AK26
A47	VSS_173	AK28
A48	VSS_174	AK29
AA12	VSS_175	AK30
AA13	VSS_176	AK32
AA30	VSS_177	AK33
AA32	VSS_178	AK35
AA35	VSS_179	AK38
AA37	VSS_180	AK45
AA39	VSS_181	AK5
AA39	VSS_182	AL19
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AA39	VSS_236	AV5
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AA39	VSS_238	AW24
AA39	VSS_239	

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UH1I		
9 OF 9		
AW25	VSS_1	F42
AW39	VSS_2	F8
AY25	VSS_3	F8
AY43	VSS_4	G1
AY5	VSS_5	G41
AY7	VSS_6	G48
B1	VSS_7	G49
B2	VSS_8	G9
B4	VSS_9	H25
B46	VSS_10	H43
B48	VSS_11	H8
B49	VSS_12	J11
B6	VSS_13	J25
BA41	VSS_14	J39
BA43	VSS_15	J9
BA49	VSS_16	K11
BA9	VSS_17	K39
BB25	VSS_18	K45
BB44	VSS_19	K5
BB8	VSS_20	L14
BC11	VSS_21	L25
BC15	VSS_22	L39
BC19	VSS_23	M12
BC24	VSS_24	M17
BC25	VSS_25	M19
BC26	VSS_26	M21
BC31	VSS_27	M22
BC35	VSS_28	M24
BC39	VSS_29	M25
BC41	VSS_30	M26
BC9	VSS_31	M28
BF1	VSS_32	M29
BF13	VSS_33	M31
BF2	VSS_34	M33
BF42	VSS_35	M38
BF46	VSS_36	M49
BF49	VSS_37	M5
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BG33	VSS_43	P38
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BG41	VSS_45	P45
BG48	VSS_46	P5
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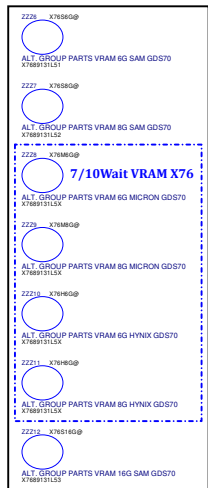
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VRAM X76:

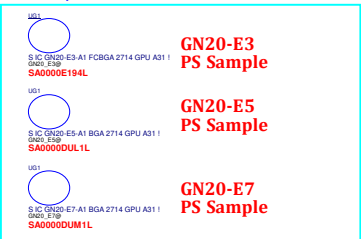


8G bit GDDR6 GN20-E3					
Micron 6G Byte		Samsung 6G Byte		Hynix 6G Byte	
R1 SA0000BND6L	R3 SA0000BND7L	R1 SA0000C625L	R3 SA0000C626L	R1 SA0000DUW0L	R3 SA0000DUW1L
UM11_V8GR1@ UM3_V8GR1@ MT6TK25M32JE-14A SA0000BND6L UM12_V8GR1@ UM4_V8GR1@ MT6TK25M32JE-14A SA0000BND6L UM9_V8GR1@ MT6TK25M32JE-14A SA0000BND6L UM10_V8GR1@ MT6TK25M32JE-14A SA0000BND6L	UM11_V8GR1@ UM3_V8GR1@ MT6TK25M32JE-14A SA0000BND7L UM12_V8GR1@ UM4_V8GR1@ MT6TK25M32JE-14A SA0000BND7L UM9_V8GR1@ MT6TK25M32JE-14A SA0000BND7L UM10_V8GR1@ MT6TK25M32JE-14A SA0000BND7L	UM11_V8GR1@ UM3_V8GR1@ K4Z8035BHC-HC14 SA0000C625L UM12_V8GR1@ UM4_V8GR1@ K4Z8035BHC-HC14 SA0000C625L UM9_V8GR1@ K4Z8035BHC-HC14 SA0000C625L UM10_V8GR1@ K4Z8035BHC-HC14 SA0000C625L	UM11_V8GR1@ UM3_V8GR1@ K4Z8035BHC-HC14 SA0000C626L UM12_V8GR1@ UM4_V8GR1@ K4Z8035BHC-HC14 SA0000C626L UM9_V8GR1@ K4Z8035BHC-HC14 SA0000C626L UM10_V8GR1@ K4Z8035BHC-HC14 SA0000C626L	UM11_V8GR1@ UM3_V8GR1@ H56C8H44A4R-S2C SA0000DUW0L UM12_V8GR1@ UM4_V8GR1@ H56C8H44A4R-S2C SA0000DUW0L UM9_V8GR1@ H56C8H44A4R-S2C SA0000DUW0L UM10_V8GR1@ H56C8H44A4R-S2C SA0000DUW0L	UM11_V8GR1@ UM3_V8GR1@ H56C8H44A4R-S2C SA0000DUW1L UM12_V8GR1@ UM4_V8GR1@ H56C8H44A4R-S2C SA0000DUW1L UM9_V8GR1@ H56C8H44A4R-S2C SA0000DUW1L UM10_V8GR1@ H56C8H44A4R-S2C SA0000DUW1L

8G bit GDDR6 GN20-E4/E5					
Micron 8G Byte		Samsung 8G Byte		Hynix 8G Byte	
R1 SA0000BND6L	R3 SA0000BND7L	R1 SA0000C625L	R3 SA0000C626L	R1 SA0000DUW0L	R3 SA0000DUW1L
UM11_V8GR1@ UM3_V8GR1@ MT6TK25M32JE-14A SA0000BND6L UM12_V8GR1@ UM4_V8GR1@ MT6TK25M32JE-14A SA0000BND6L UM9_V8GR1@ UM1_V8GR1@ MT6TK25M32JE-14A SA0000BND6L UM10_V8GR1@ UM2_V8GR1@ MT6TK25M32JE-14A SA0000BND6L	UM11_V8GR1@ UM3_V8GR1@ MT6TK25M32JE-14A SA0000BND7L UM12_V8GR1@ UM4_V8GR1@ MT6TK25M32JE-14A SA0000BND7L UM9_V8GR1@ UM1_V8GR1@ MT6TK25M32JE-14A SA0000BND7L UM10_V8GR1@ UM2_V8GR1@ MT6TK25M32JE-14A SA0000BND7L	UM11_V8GR1@ UM3_V8GR1@ K4Z8035BHC-HC14 SA0000C625L UM12_V8GR1@ UM4_V8GR1@ K4Z8035BHC-HC14 SA0000C625L UM9_V8GR1@ UM1_V8GR1@ K4Z8035BHC-HC14 SA0000C625L UM10_V8GR1@ UM2_V8GR1@ K4Z8035BHC-HC14 SA0000C625L	UM11_V8GR1@ UM3_V8GR1@ K4Z8035BHC-HC14 SA0000C626L UM12_V8GR1@ UM4_V8GR1@ K4Z8035BHC-HC14 SA0000C626L UM9_V8GR1@ UM1_V8GR1@ K4Z8035BHC-HC14 SA0000C626L UM10_V8GR1@ UM2_V8GR1@ K4Z8035BHC-HC14 SA0000C626L	UM11_V8GR1@ UM3_V8GR1@ H56C8H44A4R-S2C SA0000DUW0L UM12_V8GR1@ UM4_V8GR1@ H56C8H44A4R-S2C SA0000DUW0L UM9_V8GR1@ UM1_V8GR1@ H56C8H44A4R-S2C SA0000DUW0L UM10_V8GR1@ UM2_V8GR1@ H56C8H44A4R-S2C SA0000DUW0L	UM11_V8GR1@ UM3_V8GR1@ H56C8H44A4R-S2C SA0000DUW1L UM12_V8GR1@ UM4_V8GR1@ H56C8H44A4R-S2C SA0000DUW1L UM9_V8GR1@ UM1_V8GR1@ H56C8H44A4R-S2C SA0000DUW1L UM10_V8GR1@ UM2_V8GR1@ H56C8H44A4R-S2C SA0000DUW1L

16G bit GDDR6 GN20-E7			
Samsung 16G Byte			
R1 SA0000CRG0L	R3 SA0000CRG2L	R1 SA0000CRG0L	R3 SA0000CRG2L
UM11_V516GR1@ UM3_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG0L UM12_V516GR1@ UM4_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG0L UM9_V516GR1@ UM1_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG0L UM10_V516GR1@ UM2_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG0L	UM11_V516GR1@ UM3_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG2L UM12_V516GR1@ UM4_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG2L UM9_V516GR1@ UM1_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG2L UM10_V516GR1@ UM2_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG2L	UM11_V516GR1@ UM3_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG0L UM12_V516GR1@ UM4_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG0L UM9_V516GR1@ UM1_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG0L UM10_V516GR1@ UM2_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG0L	UM11_V516GR1@ UM3_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG2L UM12_V516GR1@ UM4_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG2L UM9_V516GR1@ UM1_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG2L UM10_V516GR1@ UM2_V516GR1@ K4ZAF35B8M-HC14 SA0000CRG2L

1/6 DVT2 Modify



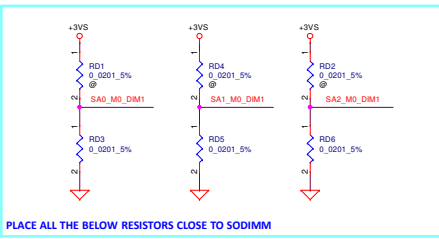
Diff 15'

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Issued Date	2020/03/27	Discontinued Date	2021/12/31	Ver	
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				Rev	0.3
				Printed	Thursday, February 18, 2021 10:08 22 of 121

CHANNEL-M0
Interleaved Memory

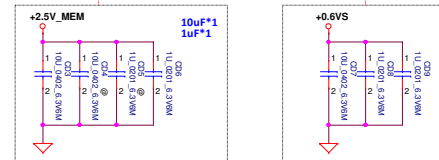
"17 ONLY" Diff 15'

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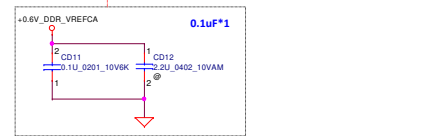


SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0xA0
READ ADDRESS: 0xA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 OPERATING SPEED: 2400/2666 MT/s

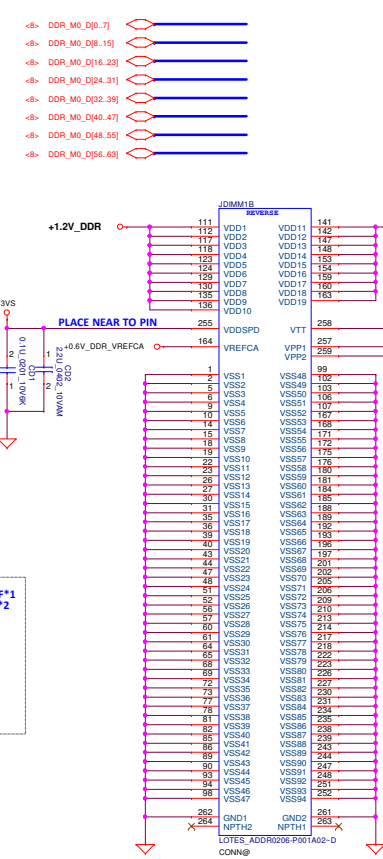
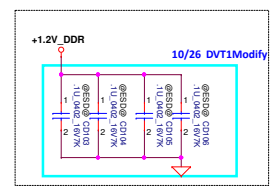
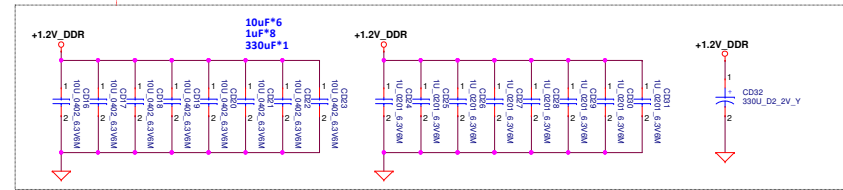
Layout Note:
Place near JDIMM1.257,259



Layout Note:
PLACE THE CAP near JDIMM1. 164

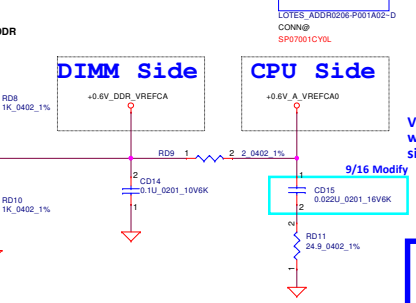
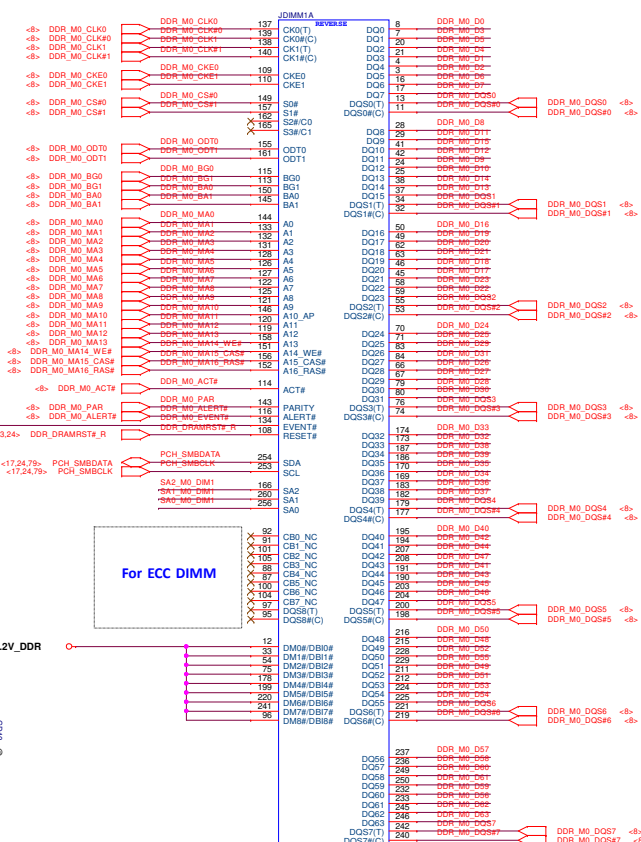


Layout Note:
Place near JDIMM1

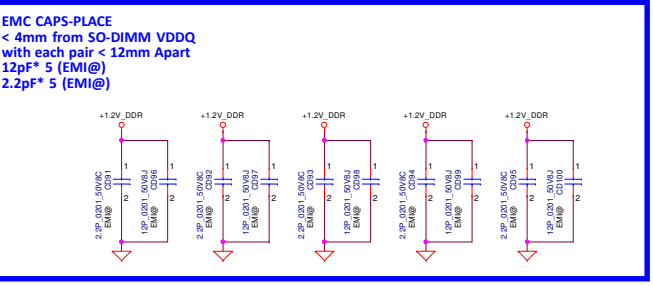


Part Number: SP07001JH00
Part Value: S SOCKET LOTES ADDR0208-P001A 260P DDR4

REVERSE TYPE (4 mm)



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

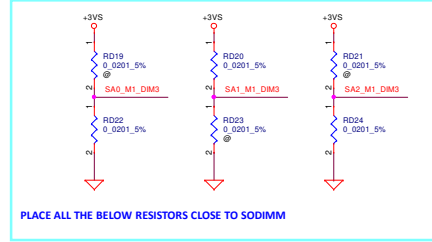


CHANNEL-M1 "17 ONLY"

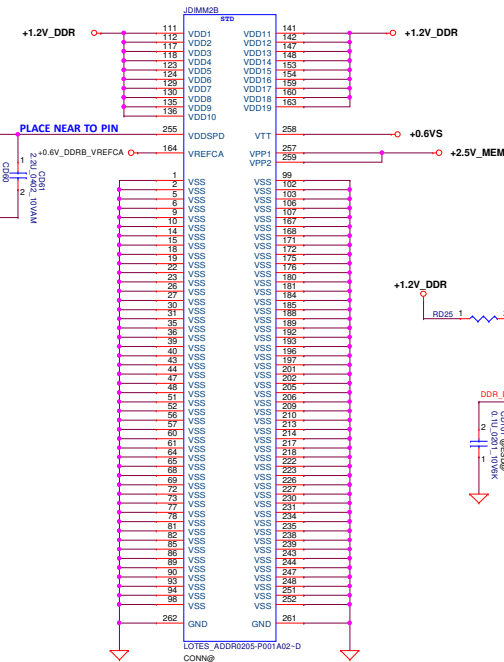
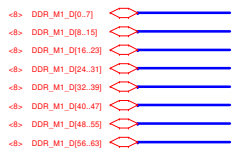
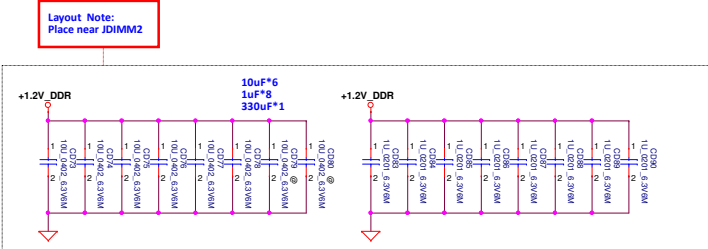
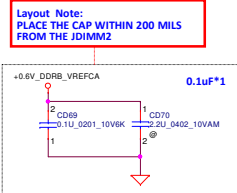
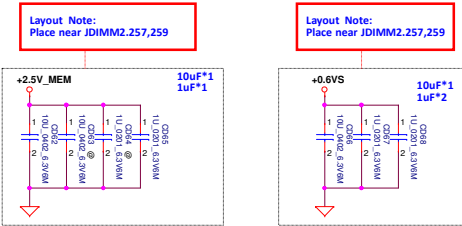
Interleaved Memory

Diff 15'

TOP: JDIMM3 CONN Non-ECC DIMM

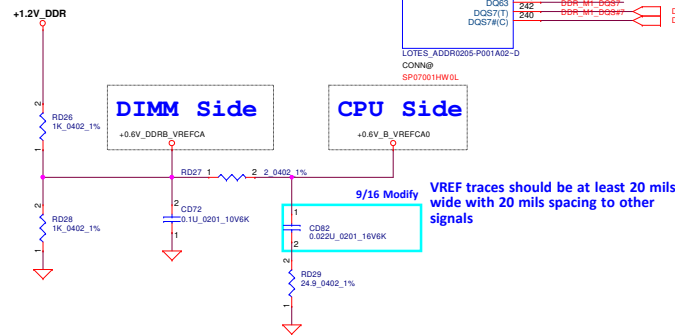
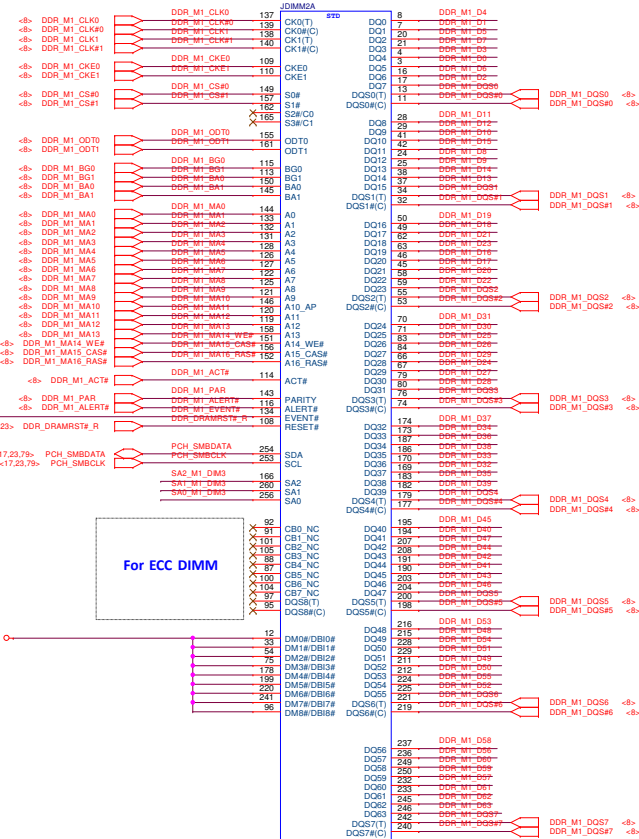


SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA2
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 OPERATING SPEED: 2400/2600 MT/S



Part Number: SP07001HY00
Part Value: S SOCKET LOTES ADDR0207-P001A 260P DDR4

STD (4 mm)

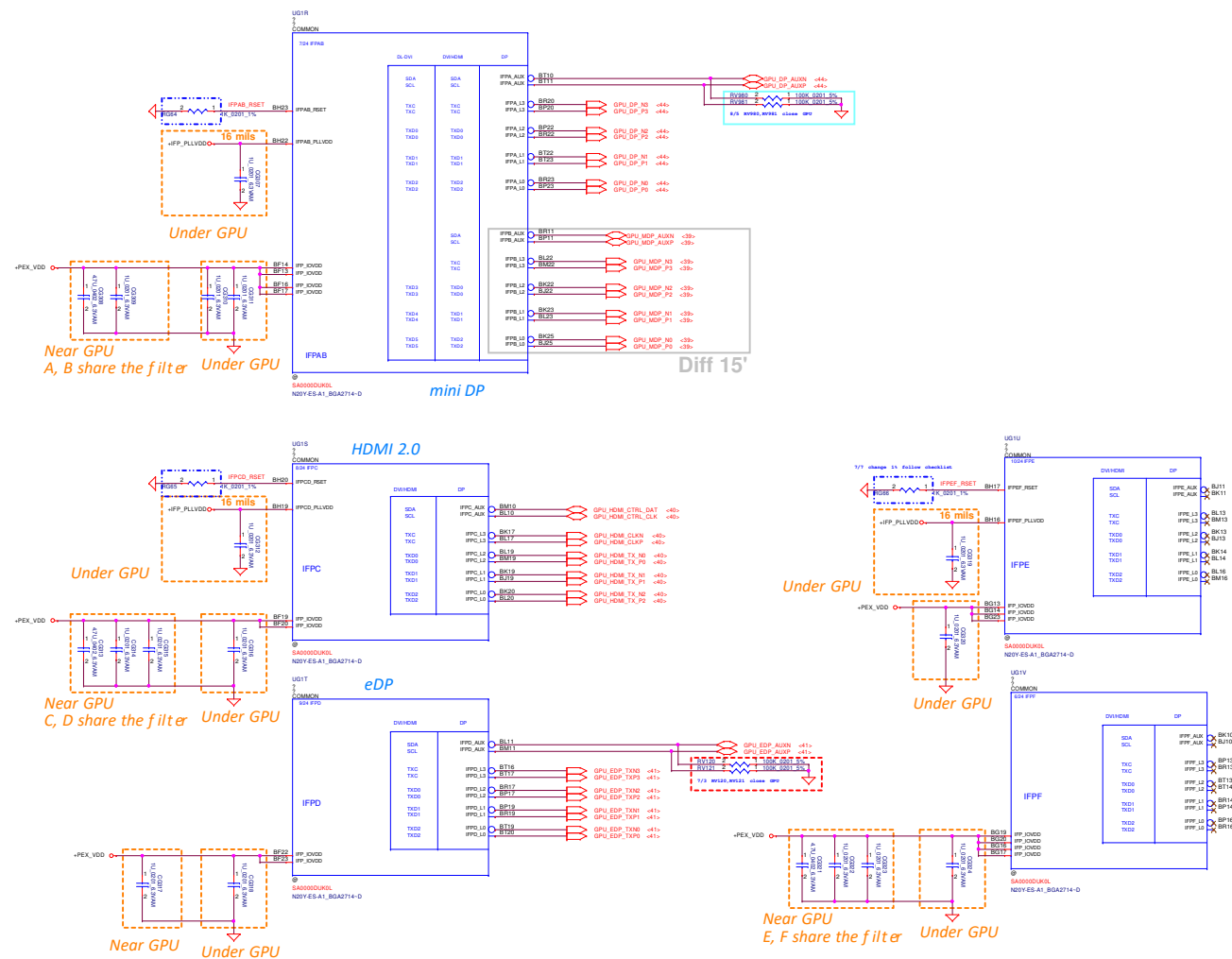


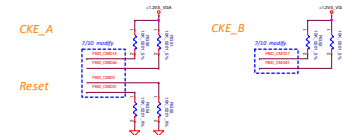
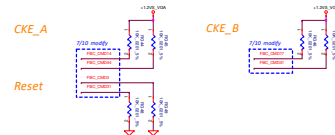
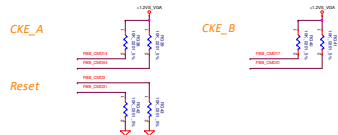
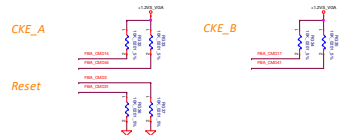
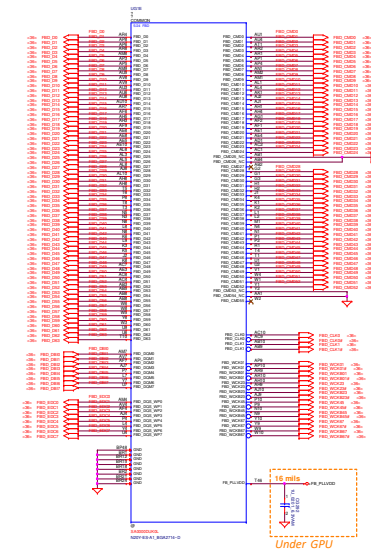
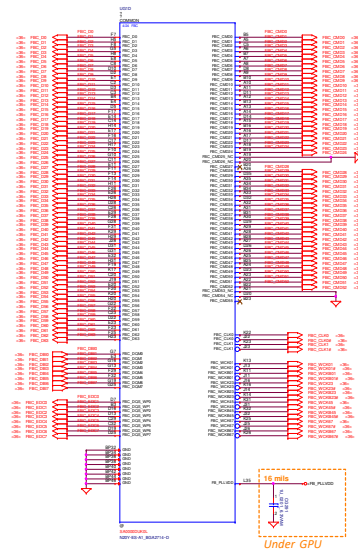
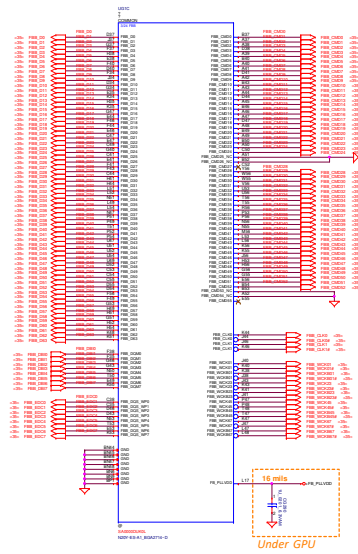
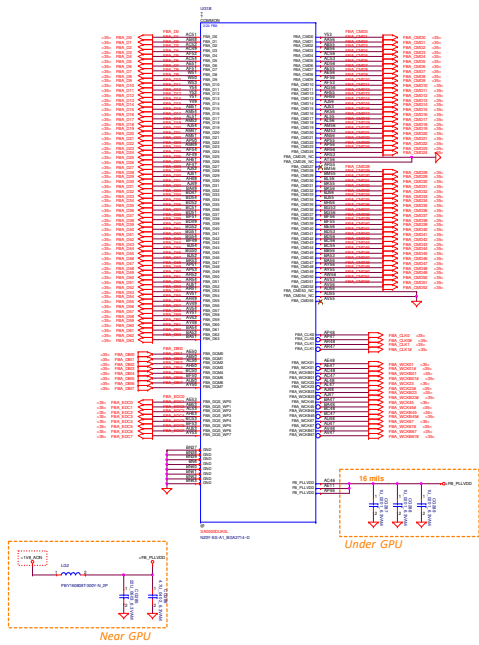
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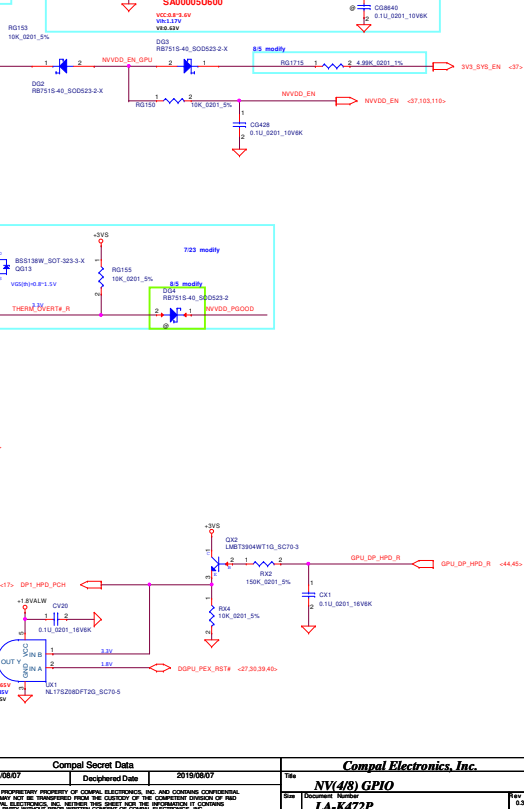
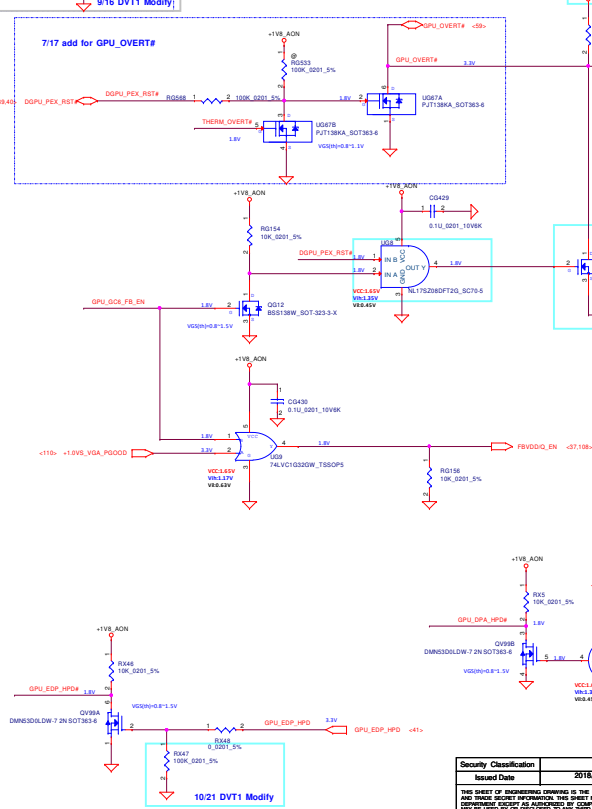
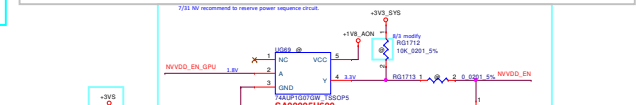
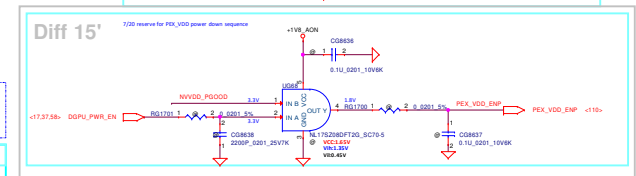
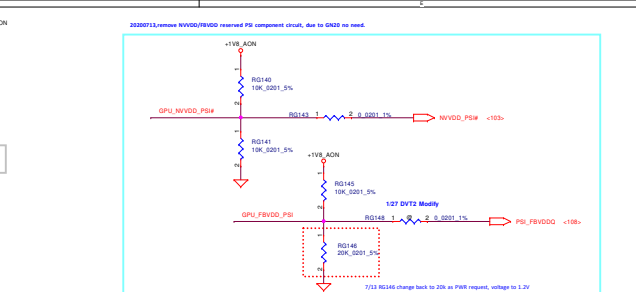
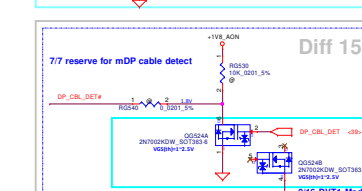
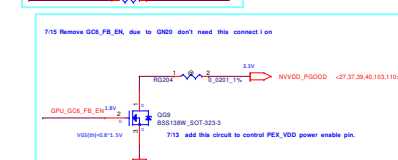
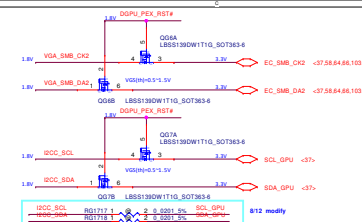
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Issued Date	2020/04/10	Deciphered Date	2021/12/31	Title	RSV
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Diff 15'

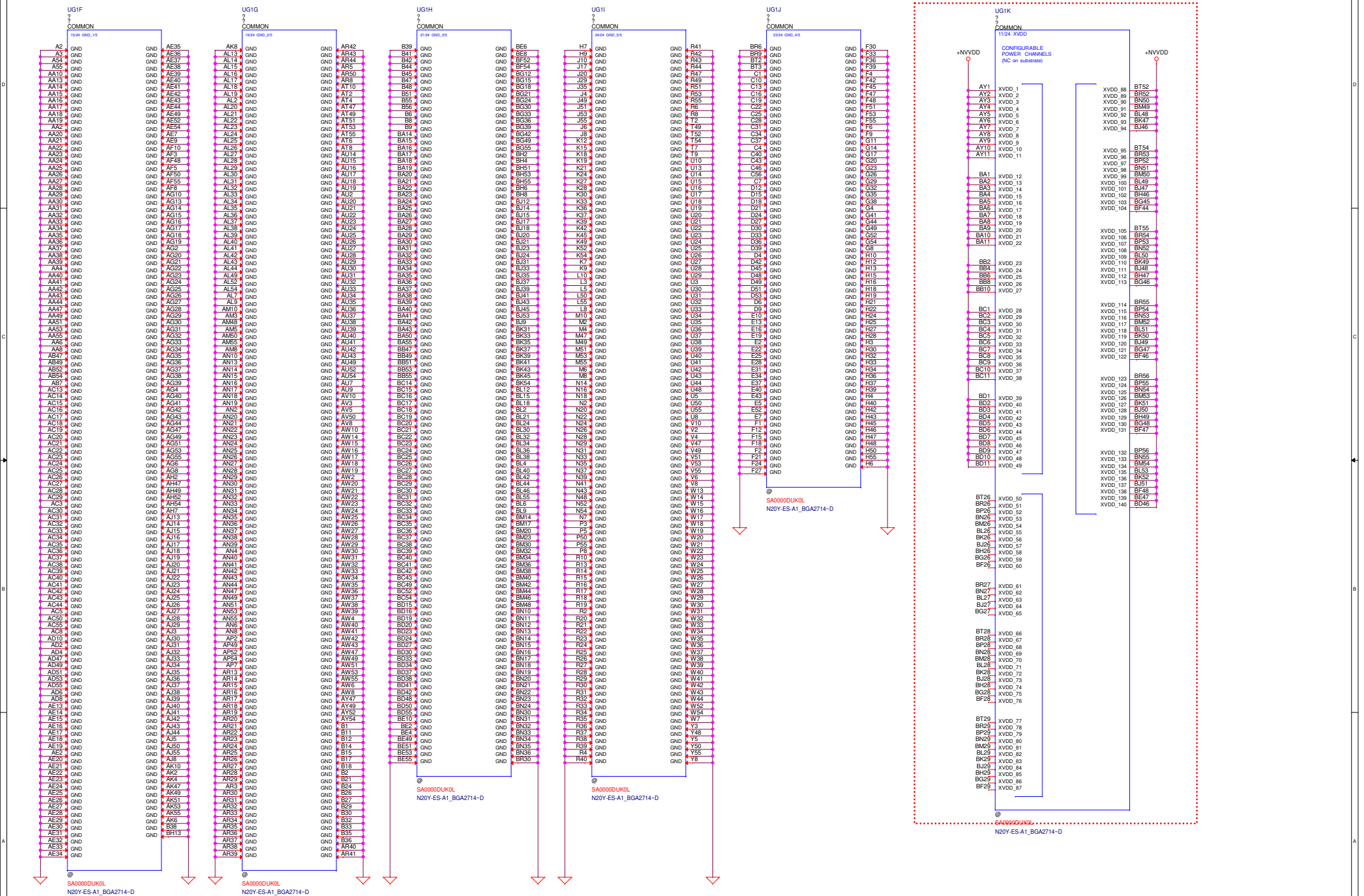
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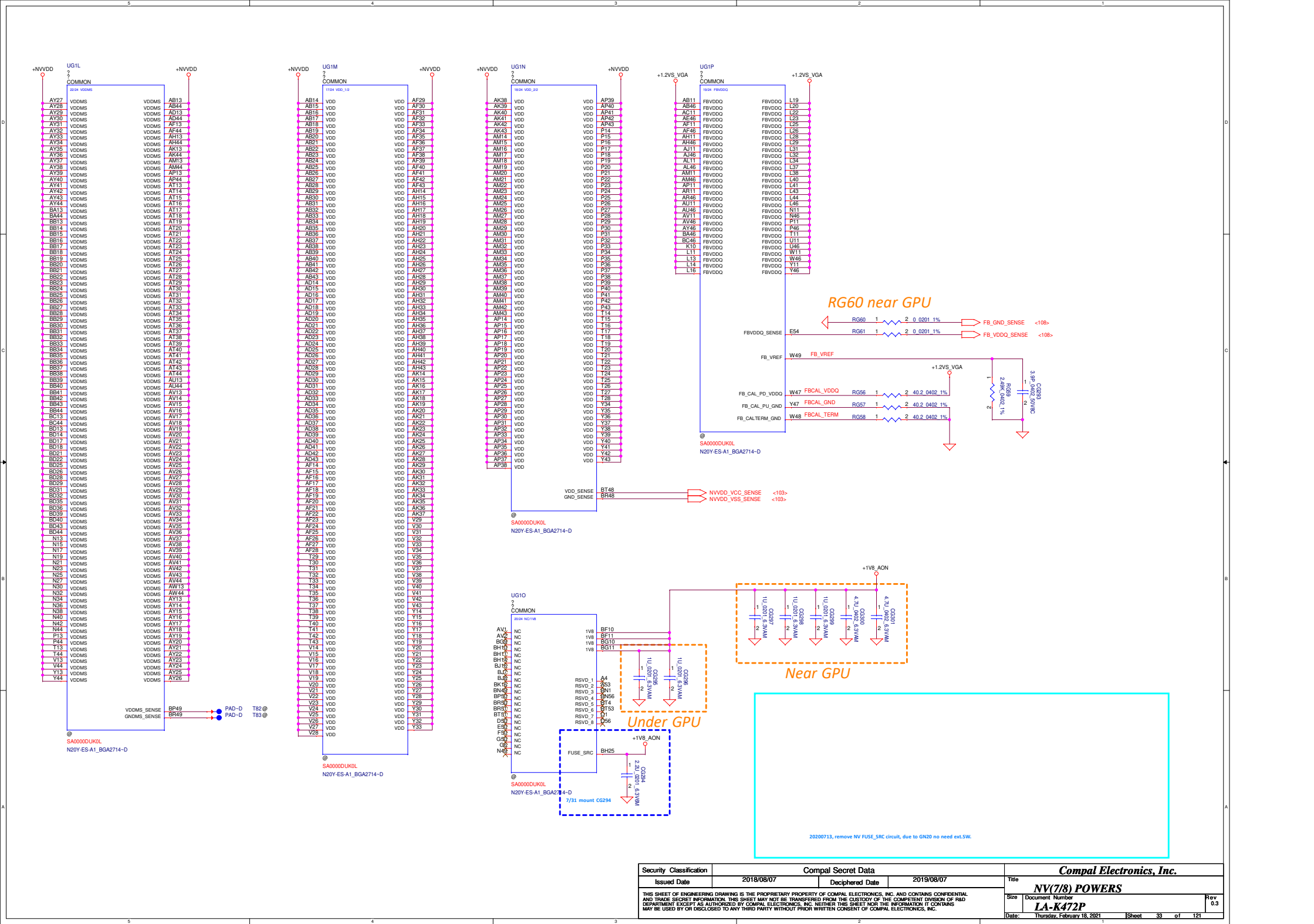




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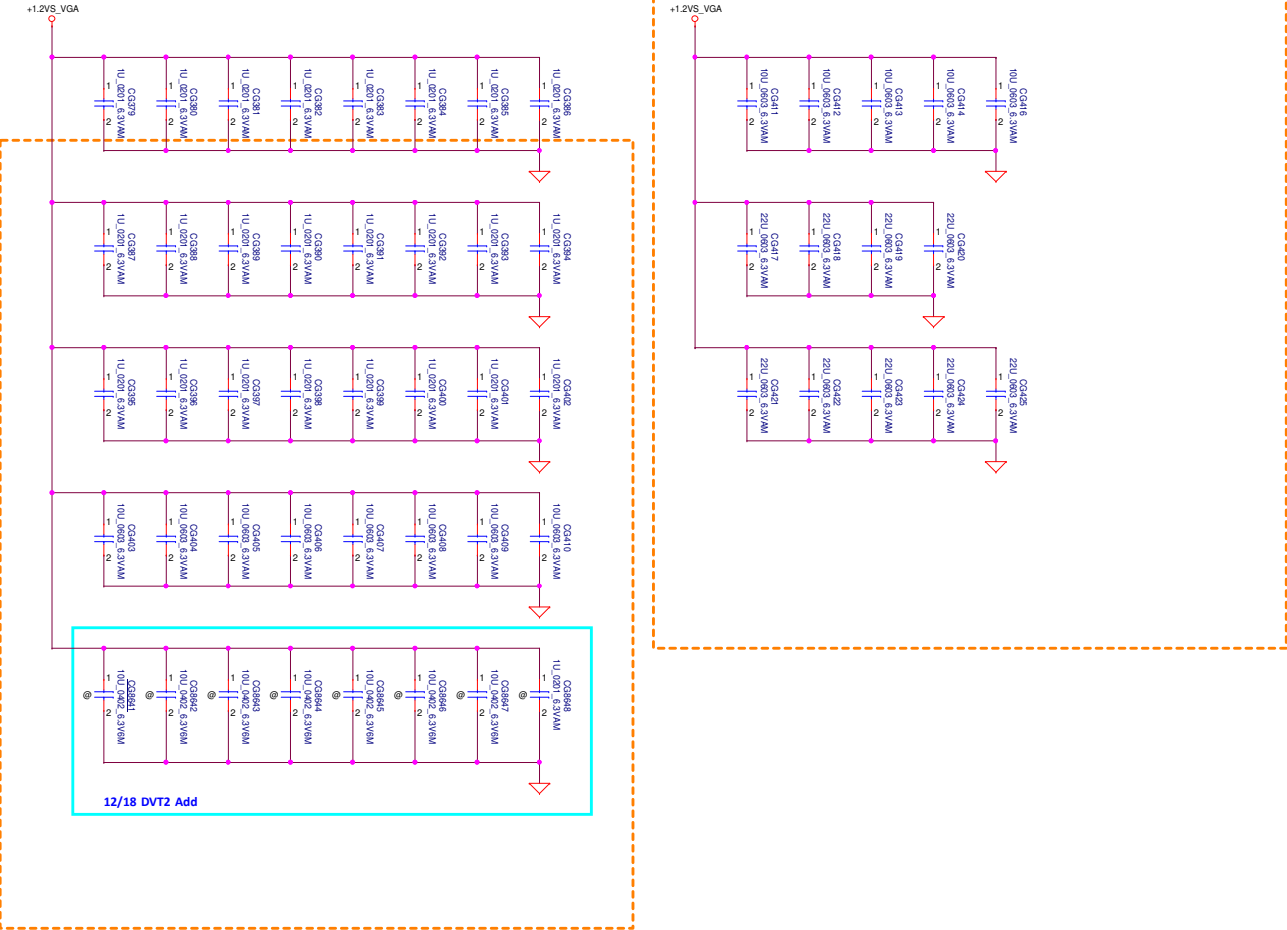
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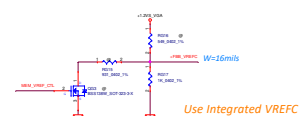
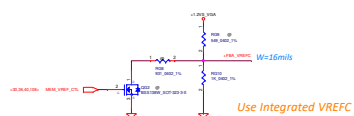
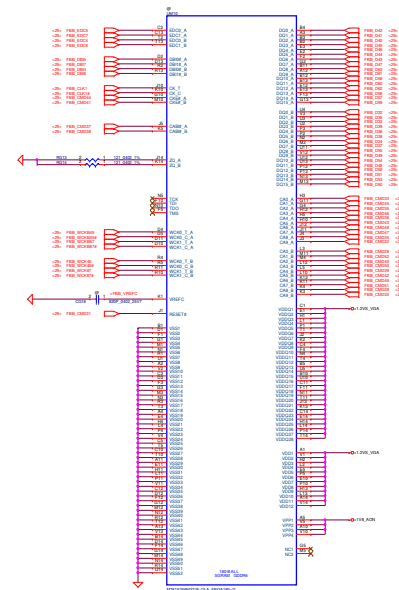
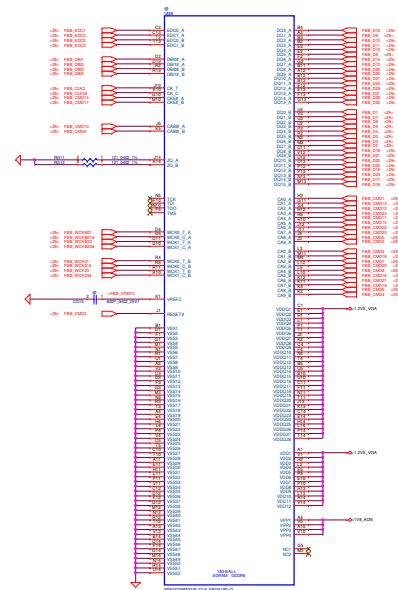
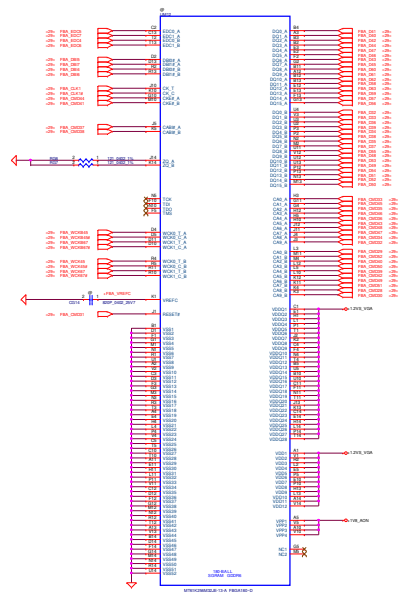
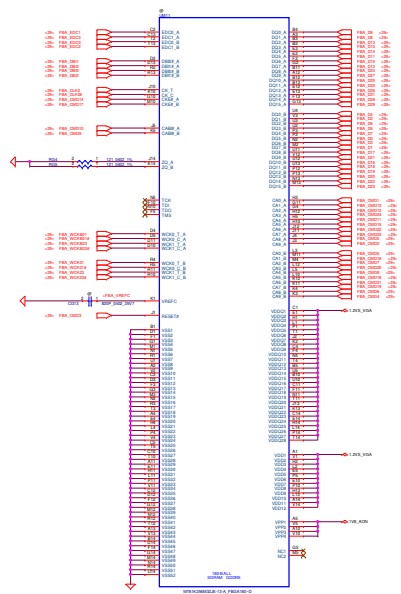


FBVDDQ_GPU

Under GPU

Near GPU





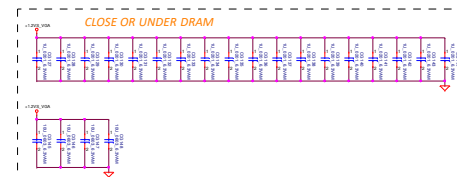
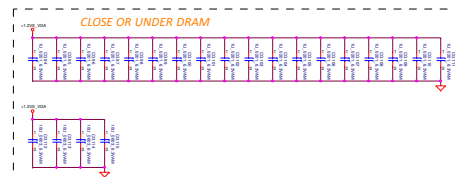
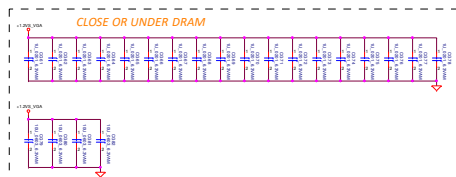
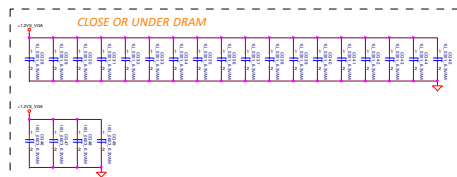
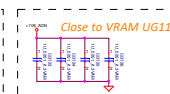
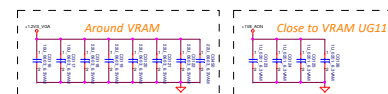
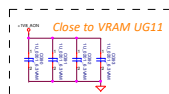
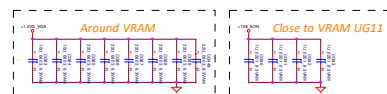
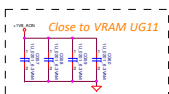
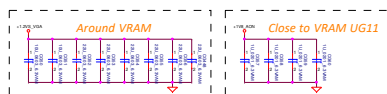
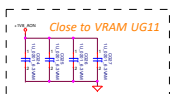
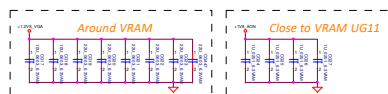
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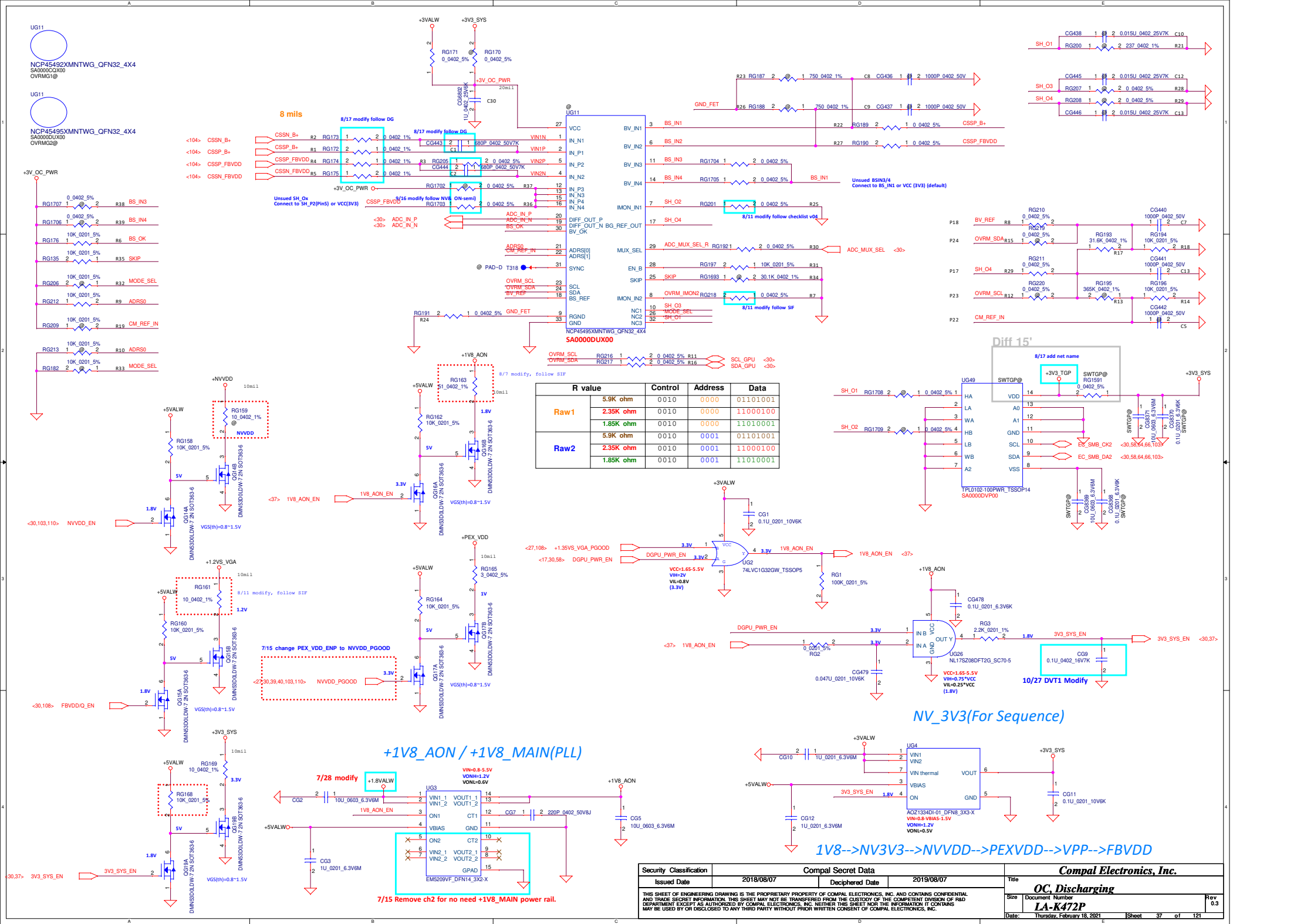
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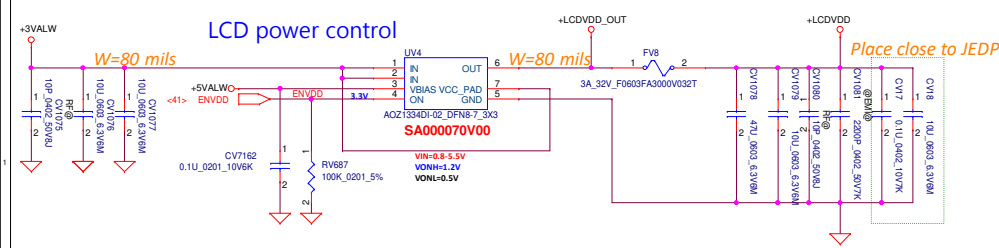
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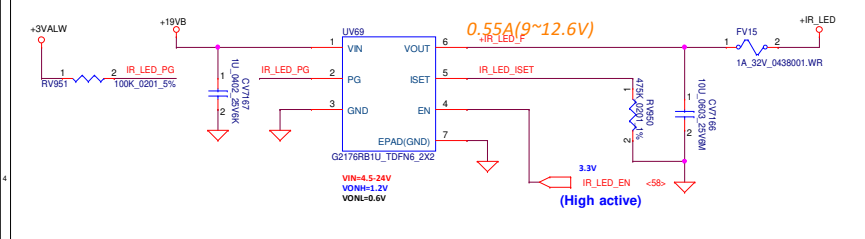
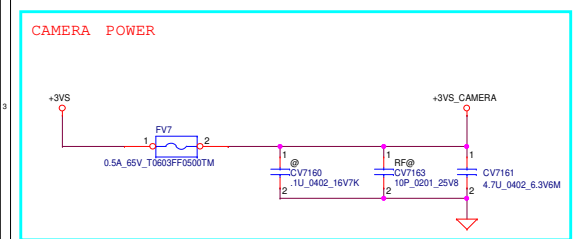
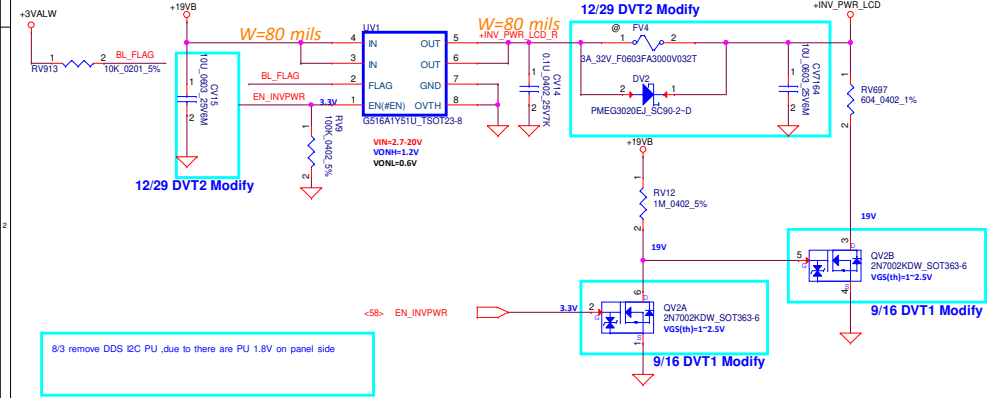


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						Size	Document Number		Rev		
						LA-K472P					0.3
						Date:	Thursday, February 18, 2021		Sheet	37	of 121

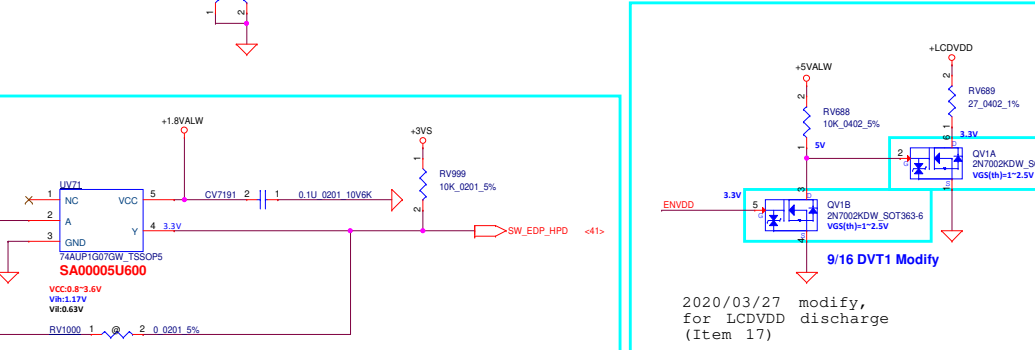
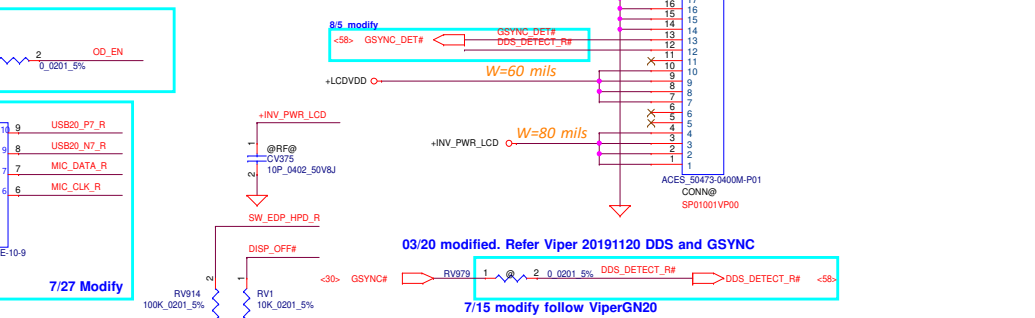
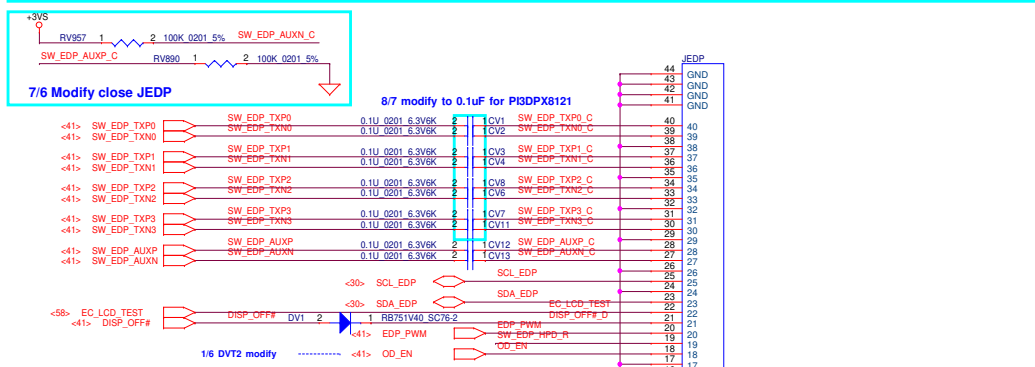
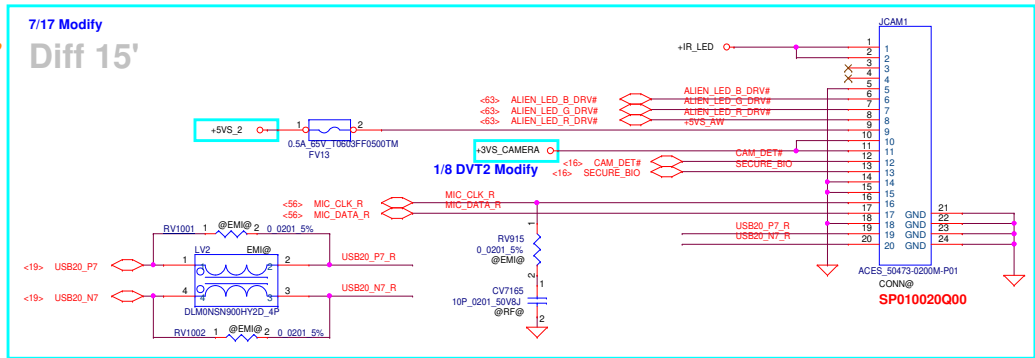
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LCD backlight power control

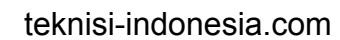


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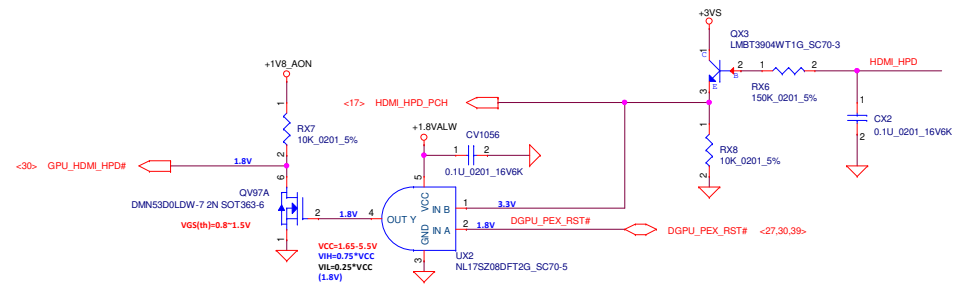
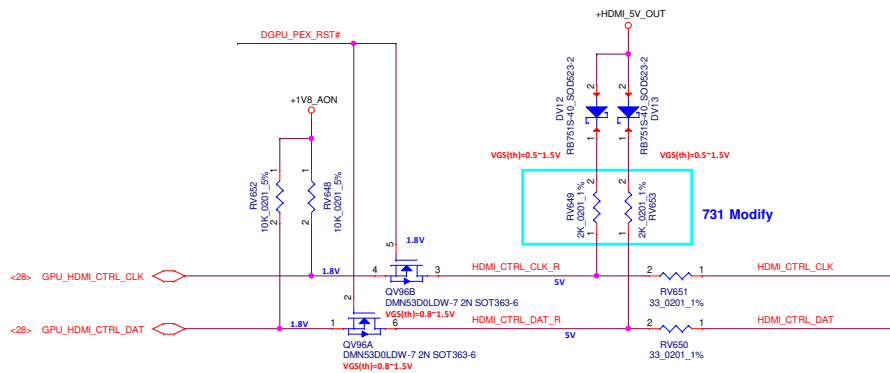
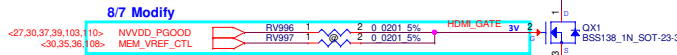
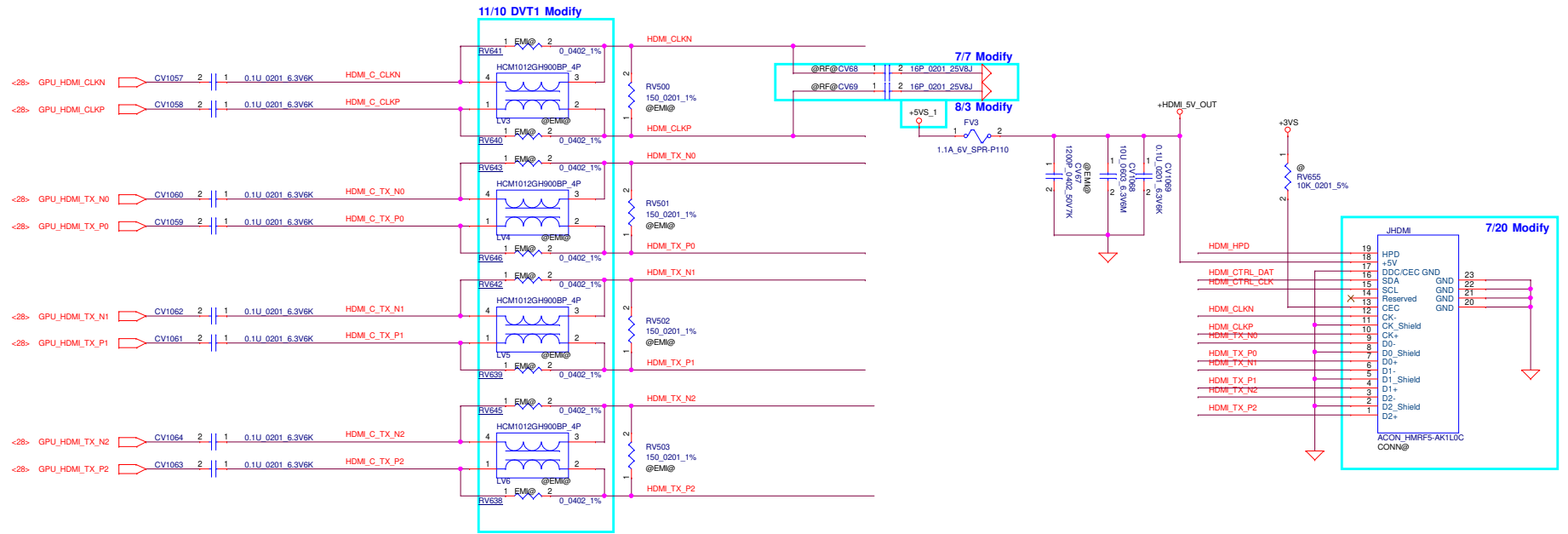


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Issued Date		Deciphered Date		eDP/Camera	
2020/02/27		2021/12/31		LA-K472P	
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Date:		Thursday, February 18, 2021		Sheet 38 of 121	

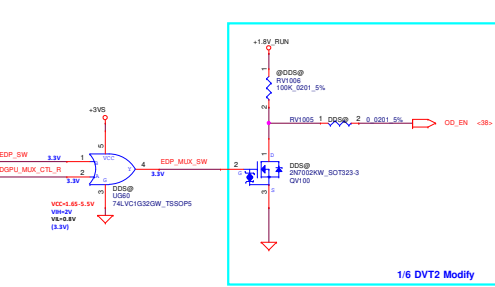
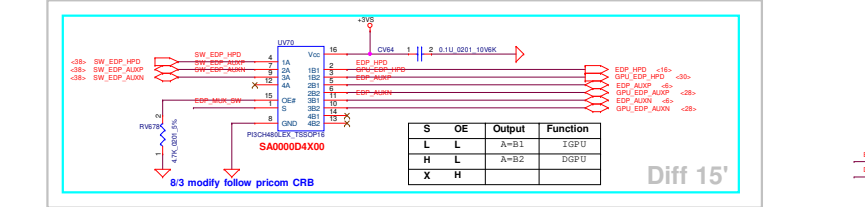
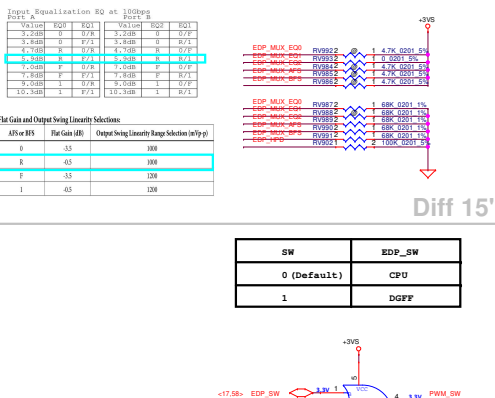
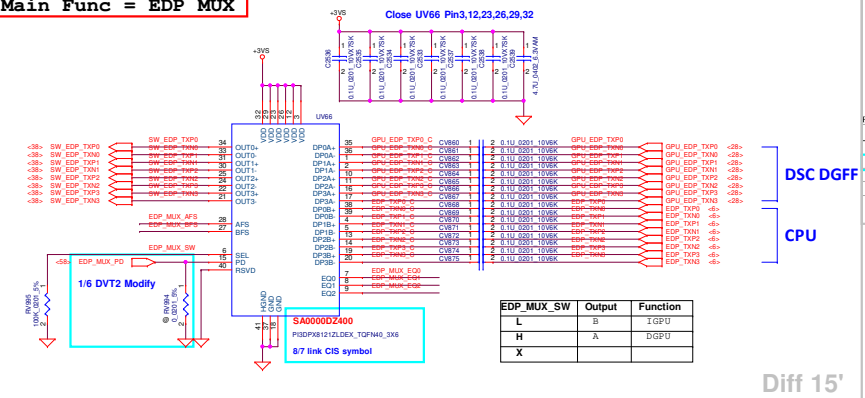
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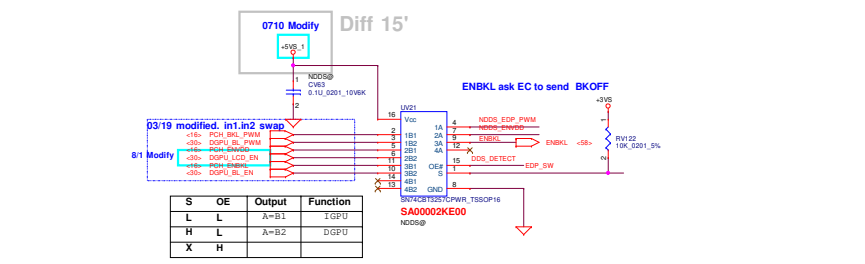
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Issued Date	2017/05/15	Deciphered Date	2018/02/05	Title	Mini DP		
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					LA-K472P	03	
				Date:	Thursday, February 18, 2021	Sheet	39 of 121



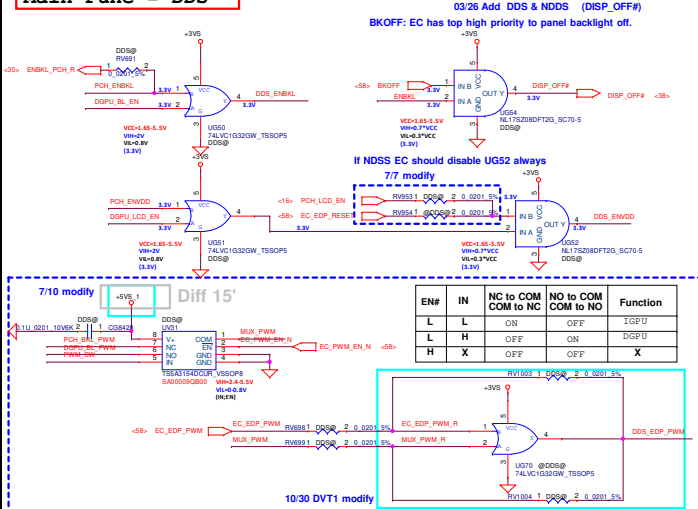
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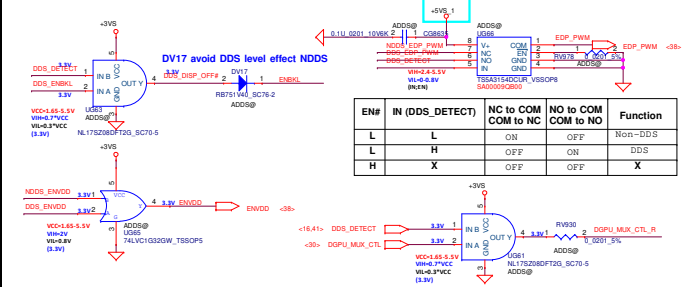
NDDS : Mshybrid mode
DDS_Detect Control close UV21



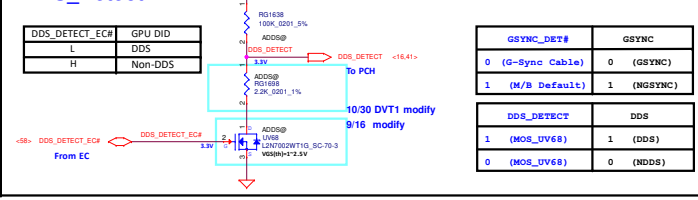
Main Func = DDS

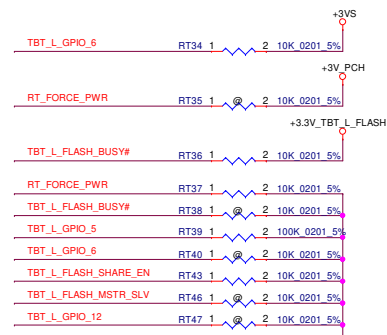
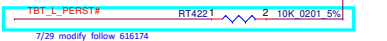
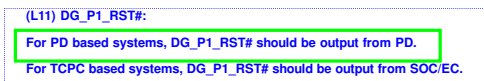
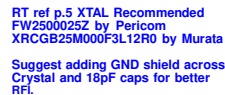
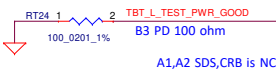
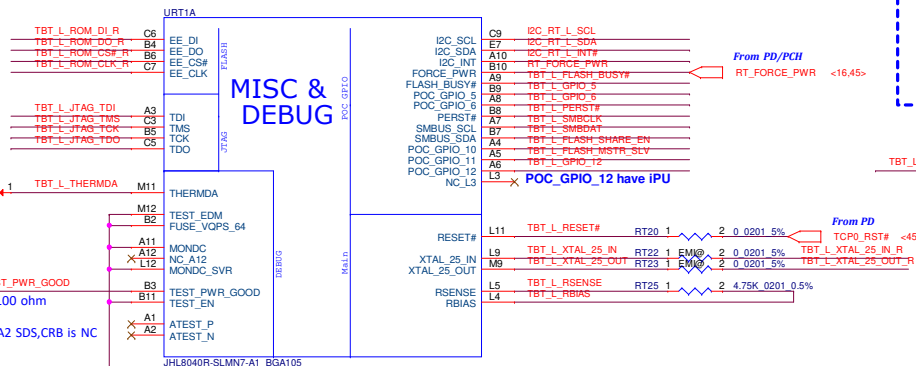
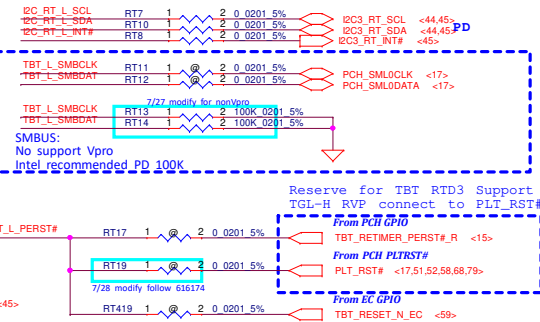


Main Func = DDS Auto Detect



DDS_Detect

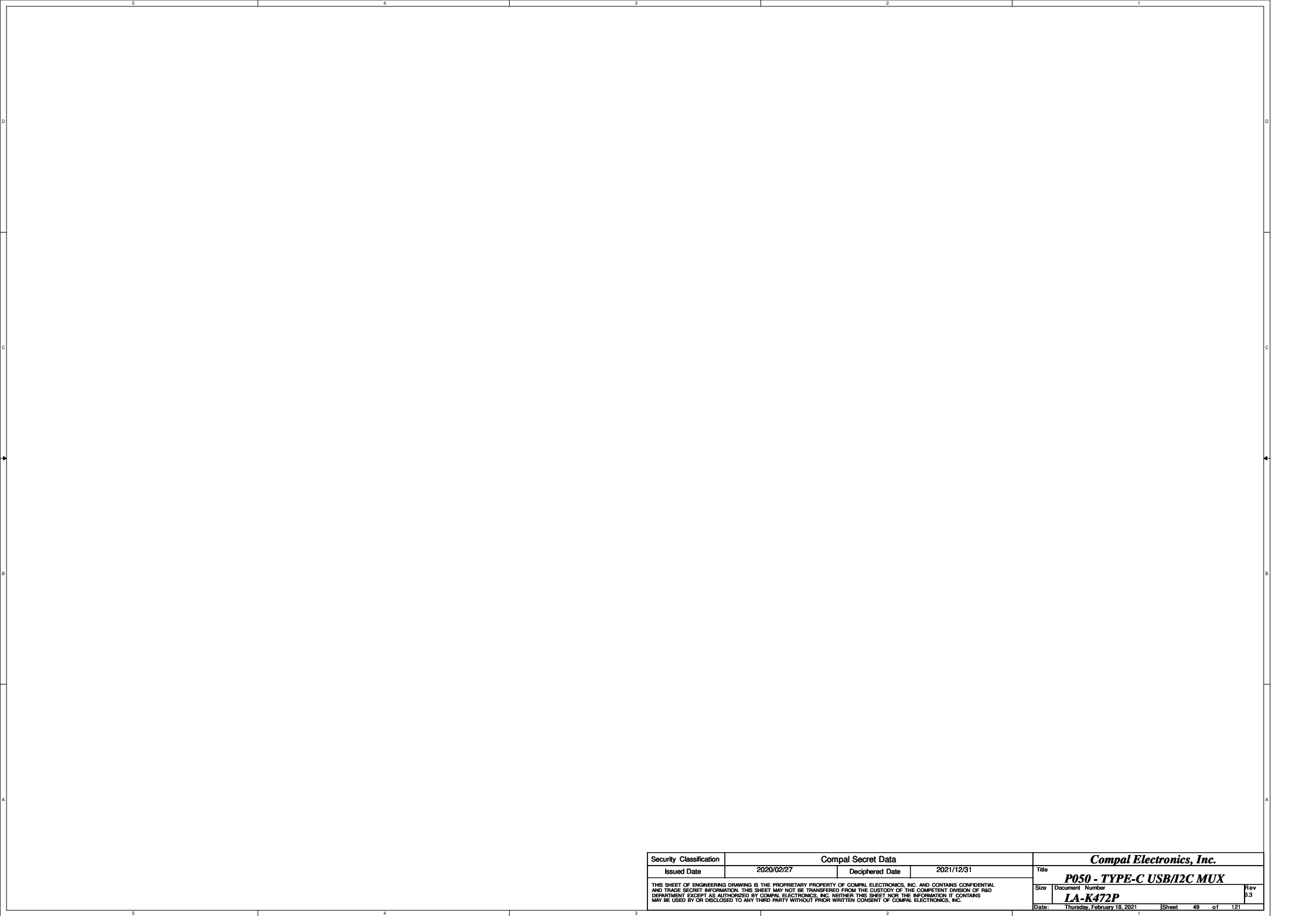




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				Date:	Thursday, February 18, 2021	Sheet 42 of 121

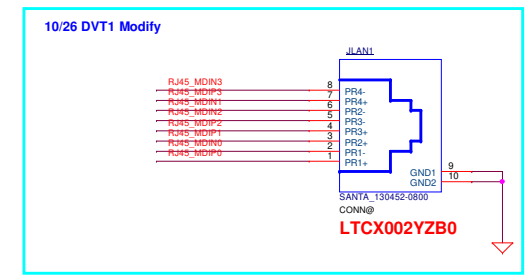
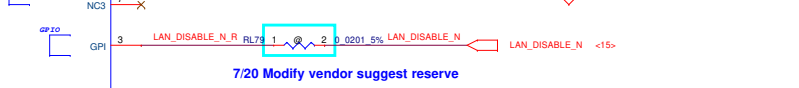
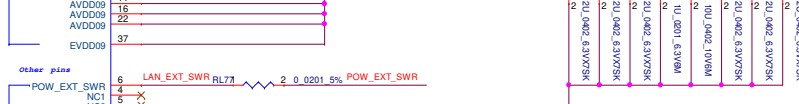
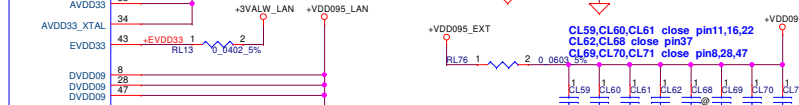
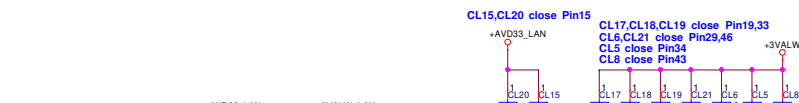
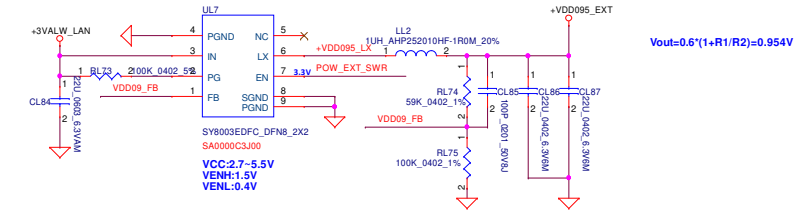
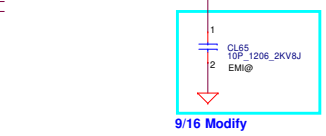
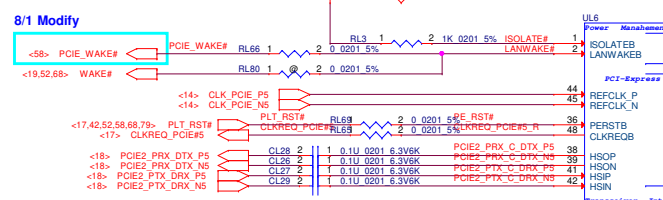
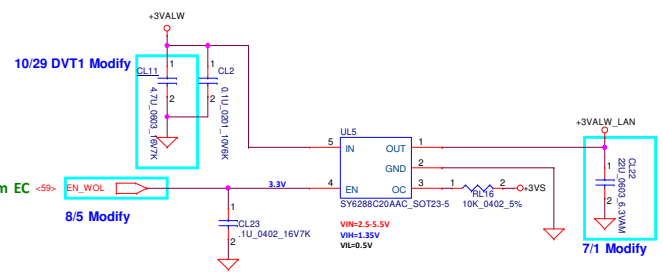
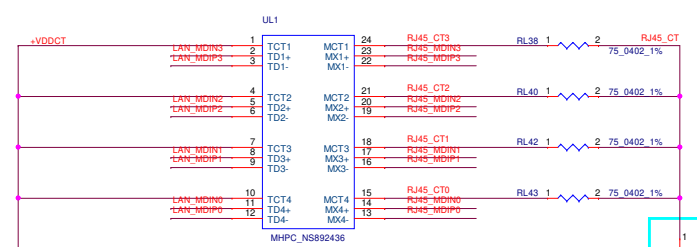
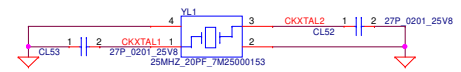
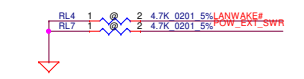
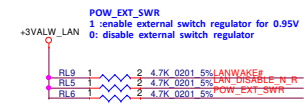
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Security Classification		Compal Secret Data		Compal Electronics, Inc.																																								
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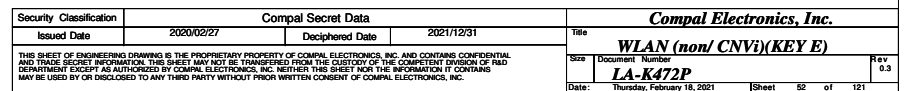
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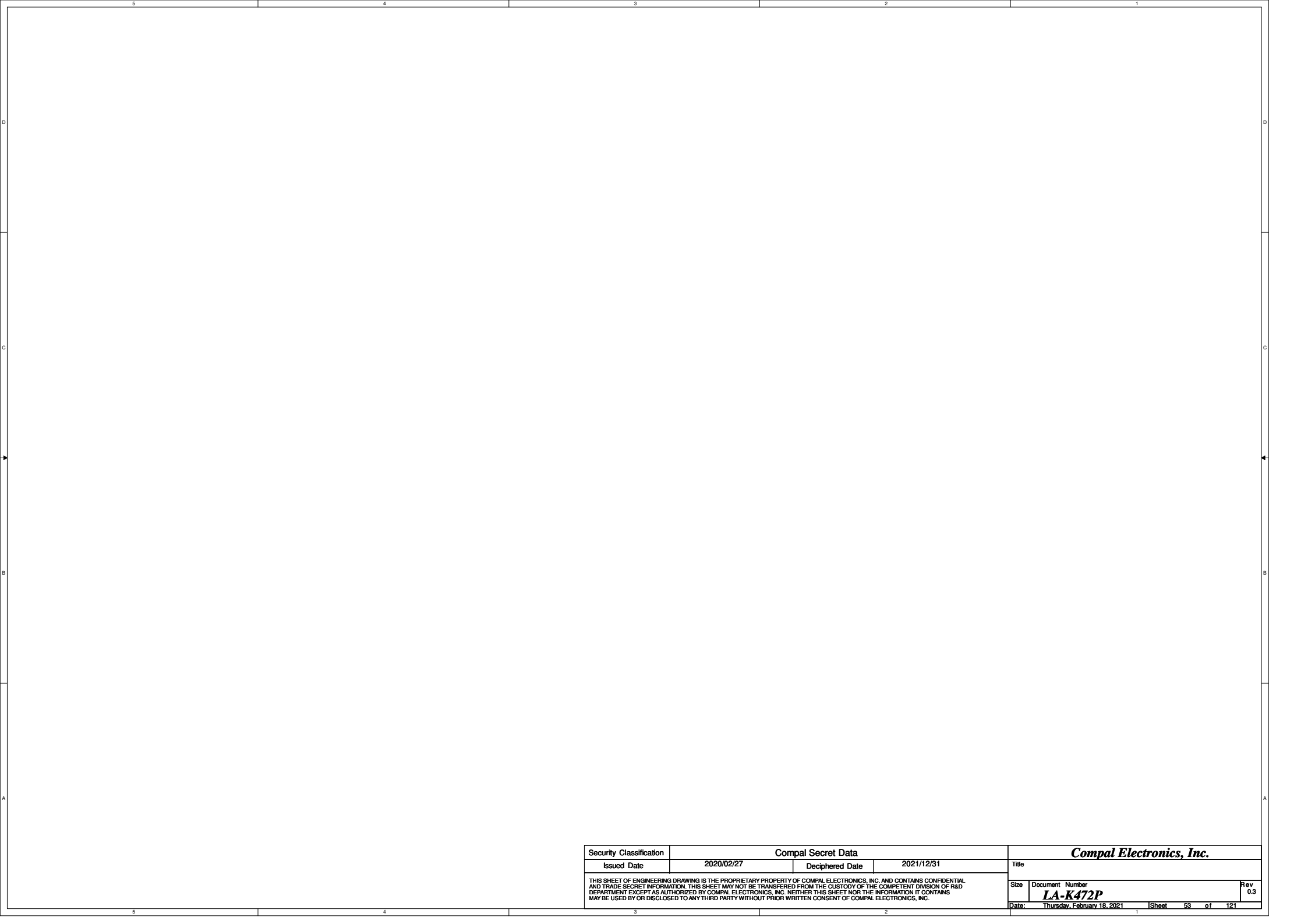
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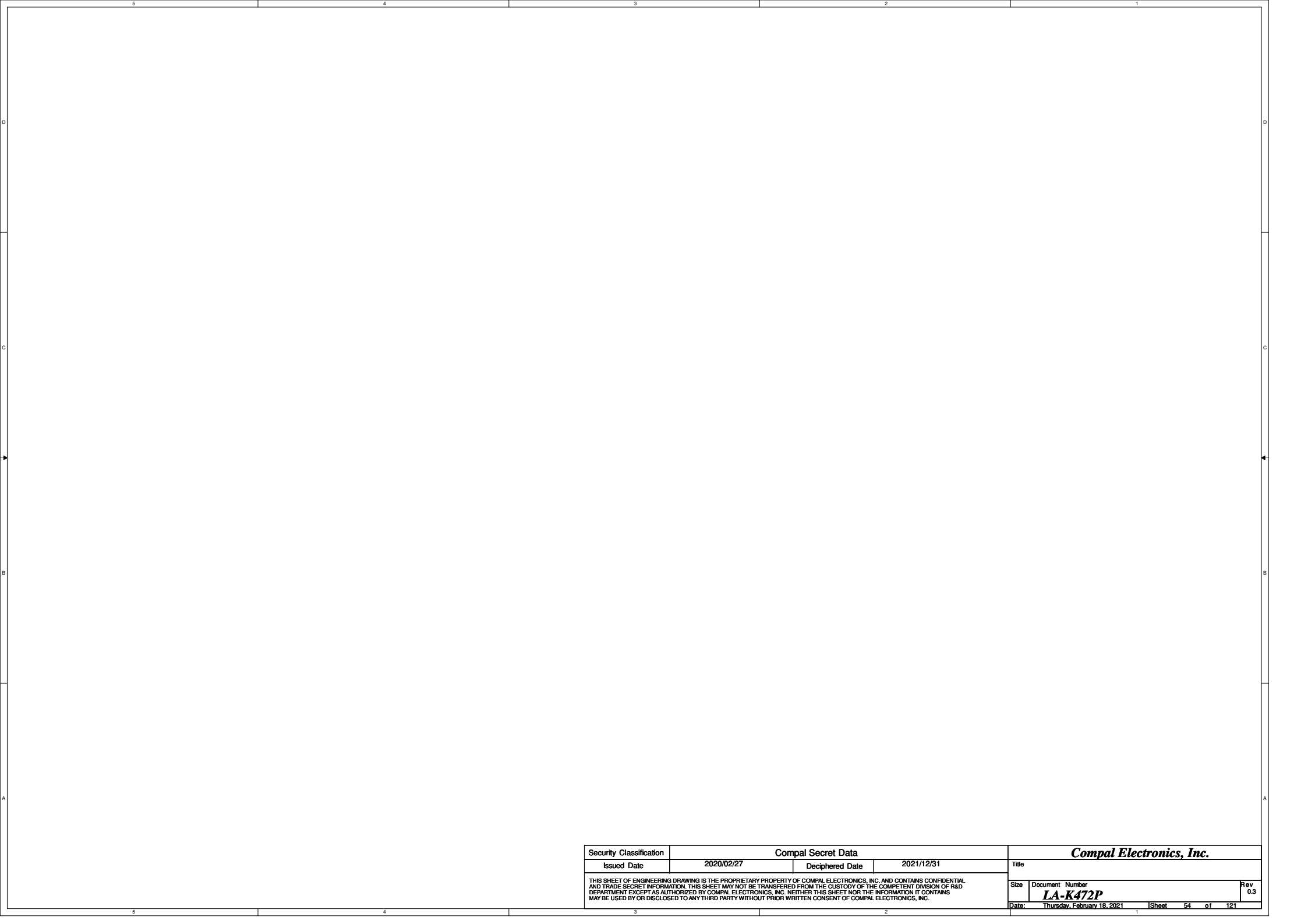
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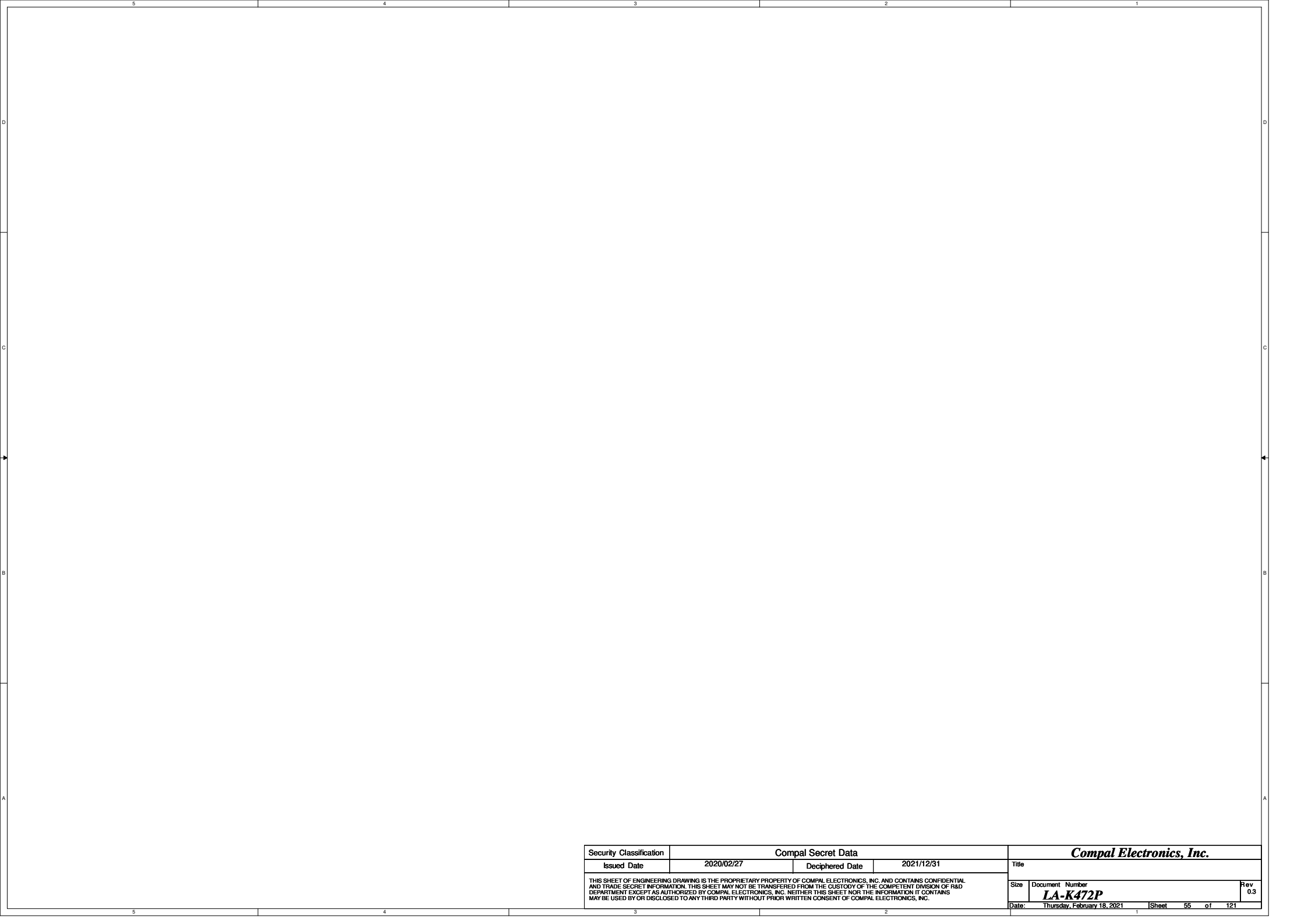




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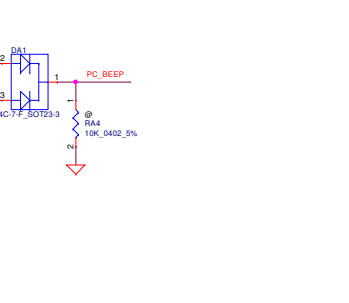
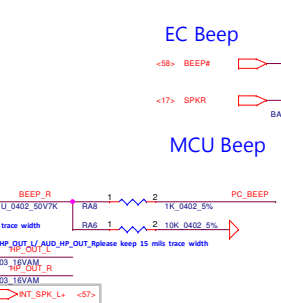
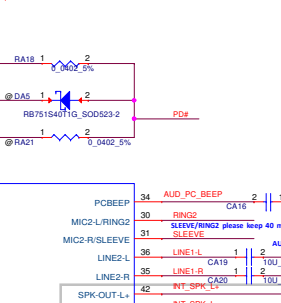
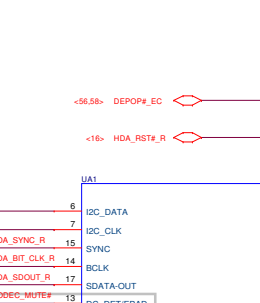
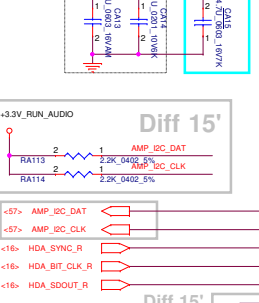
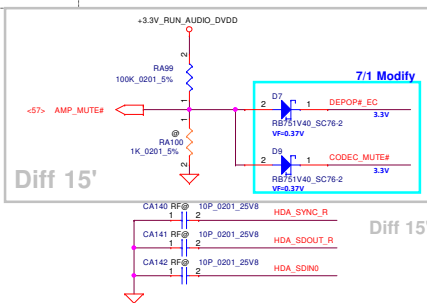
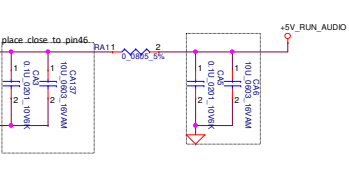
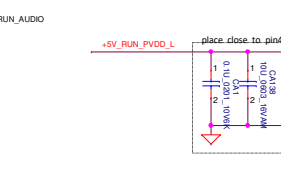
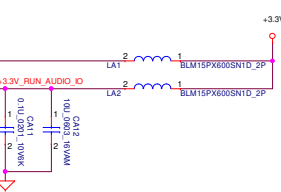
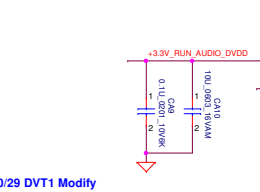
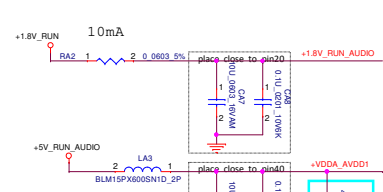
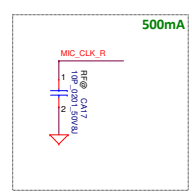
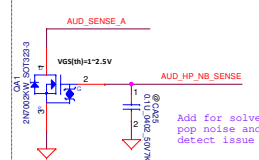


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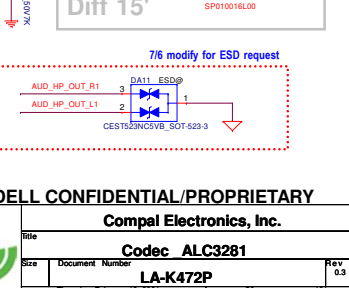
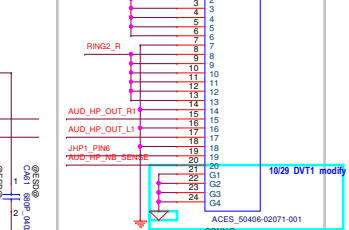
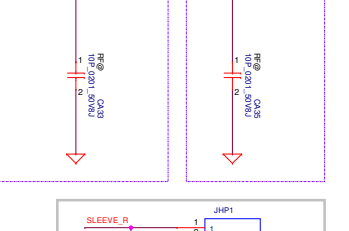
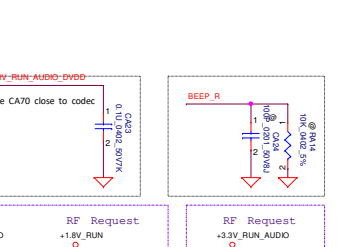
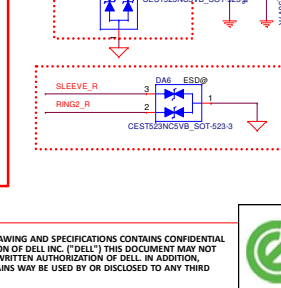
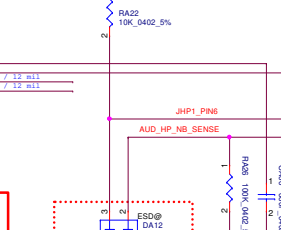
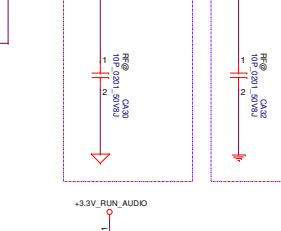
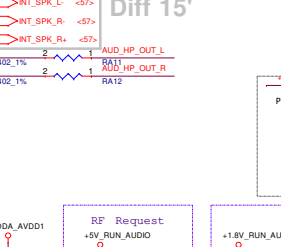
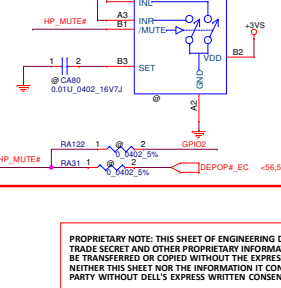
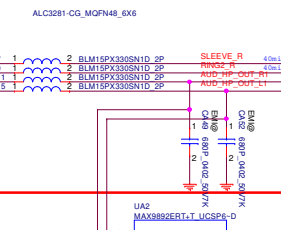
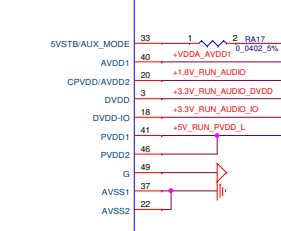
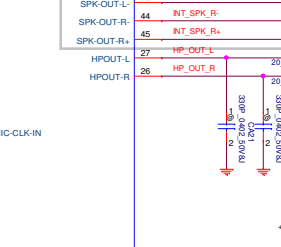
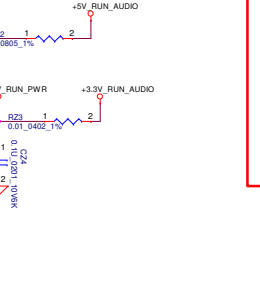
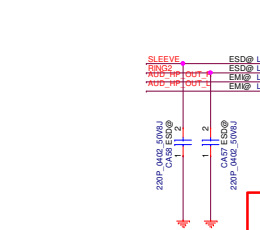
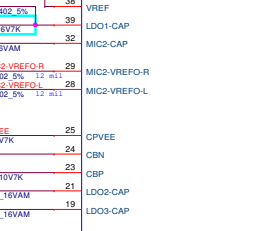
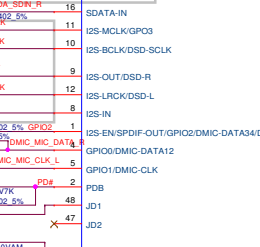
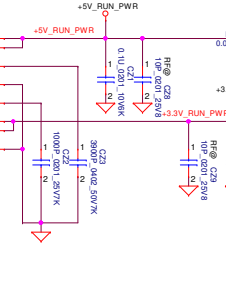
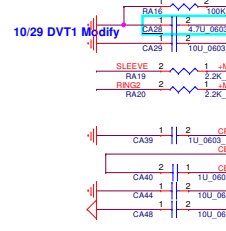
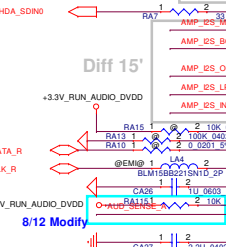
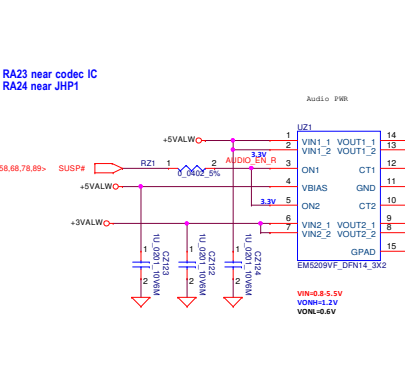
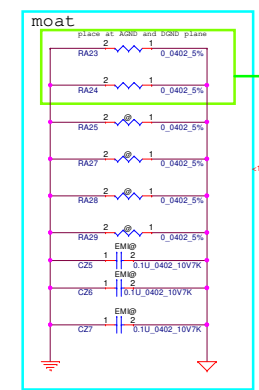
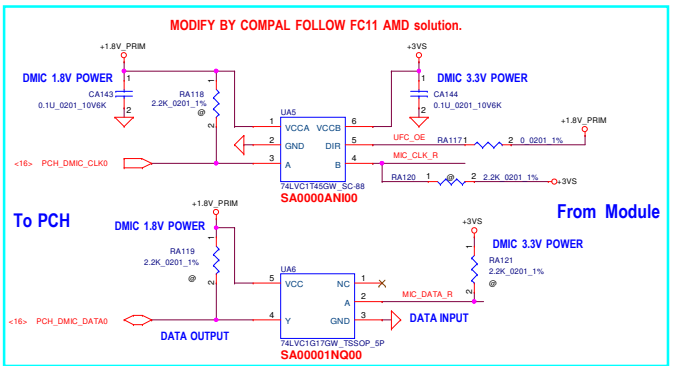
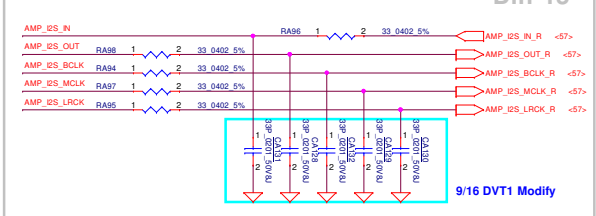


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Verb table configure as 11D mode with internal 47K pull high to save external BOM.

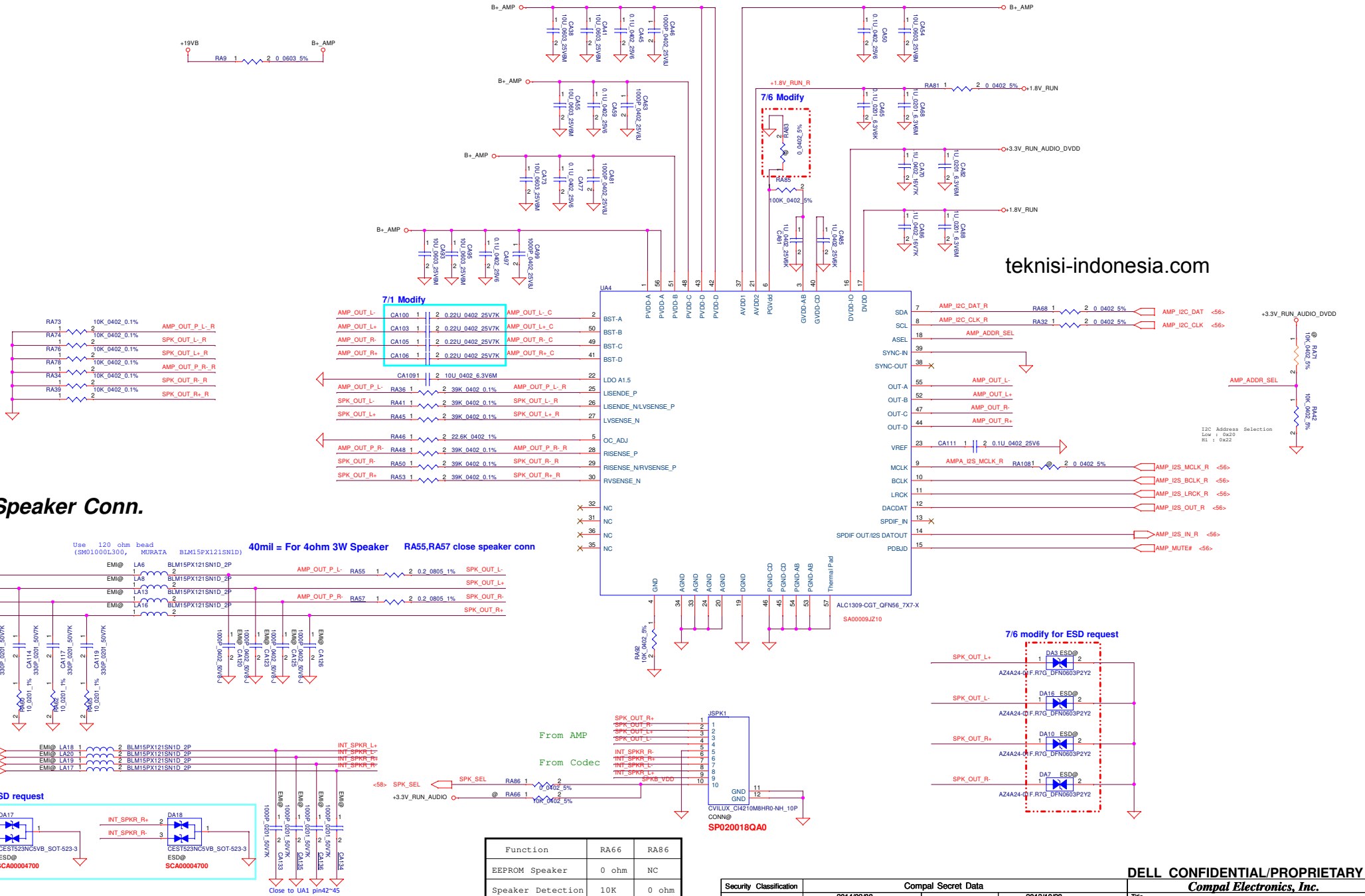


POST I2S interface



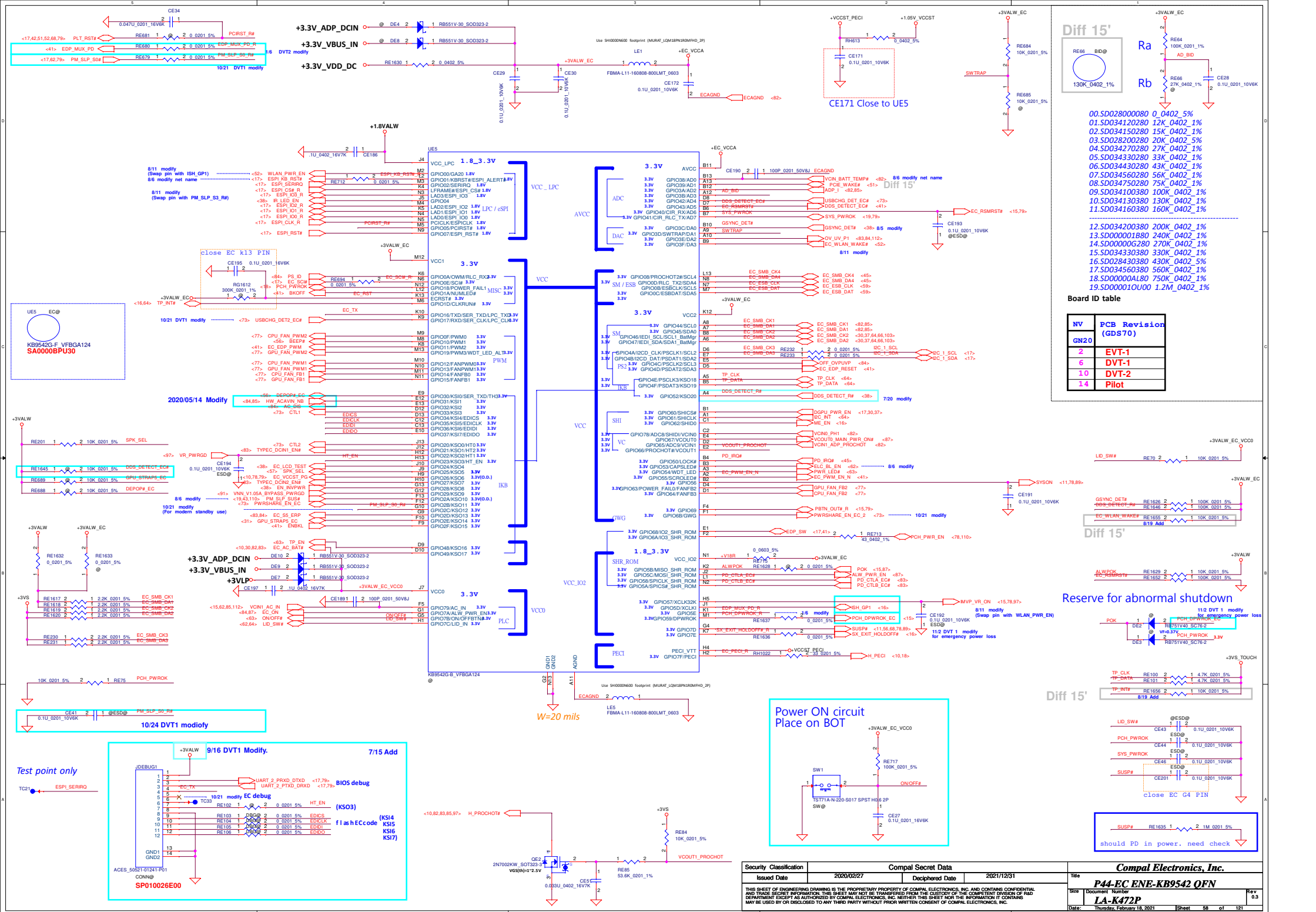
Diff 15'

teknisi-indonesia.com



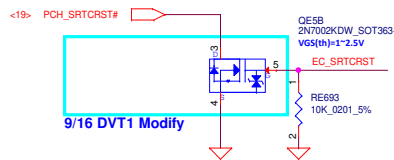
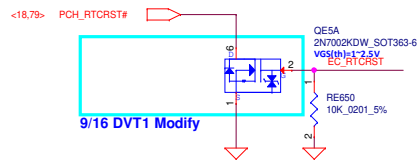
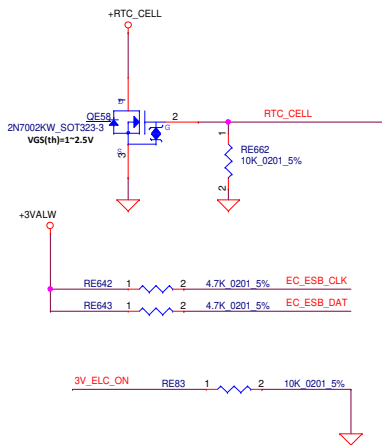
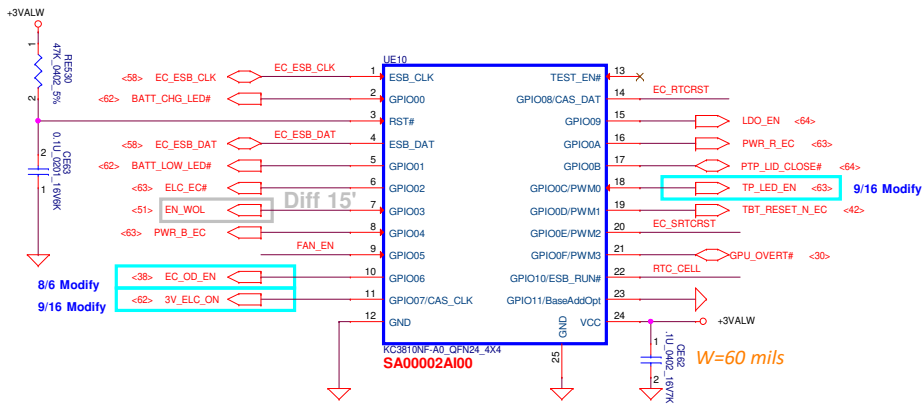
Function	RA66	RA86
EEPROM Speaker	0 ohm	NC
Speaker Detection	10K	0 ohm

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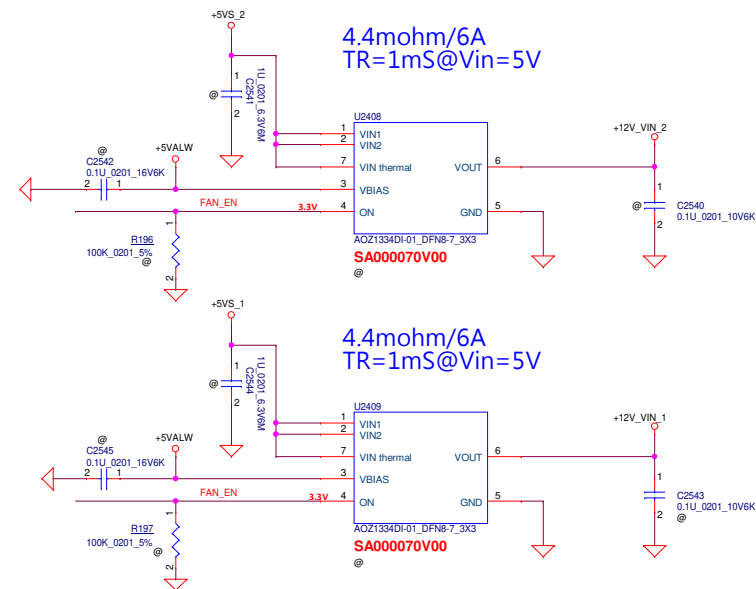
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			Date: LA-K472P	
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Main Func = EC ENE-KC3810

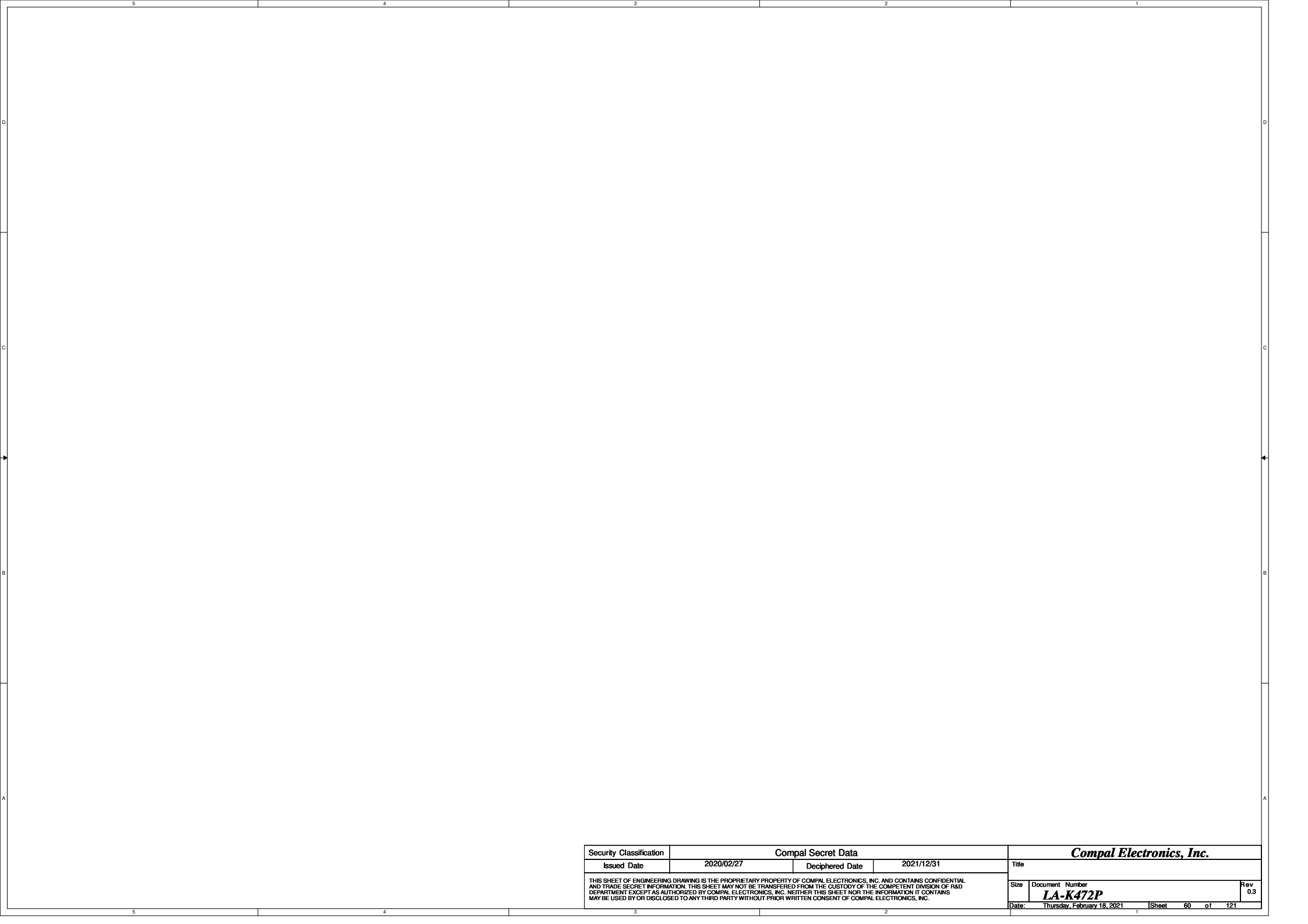


Main Func = FAN_EN (Reserve only)

"17 ONLY"
Diff 15'



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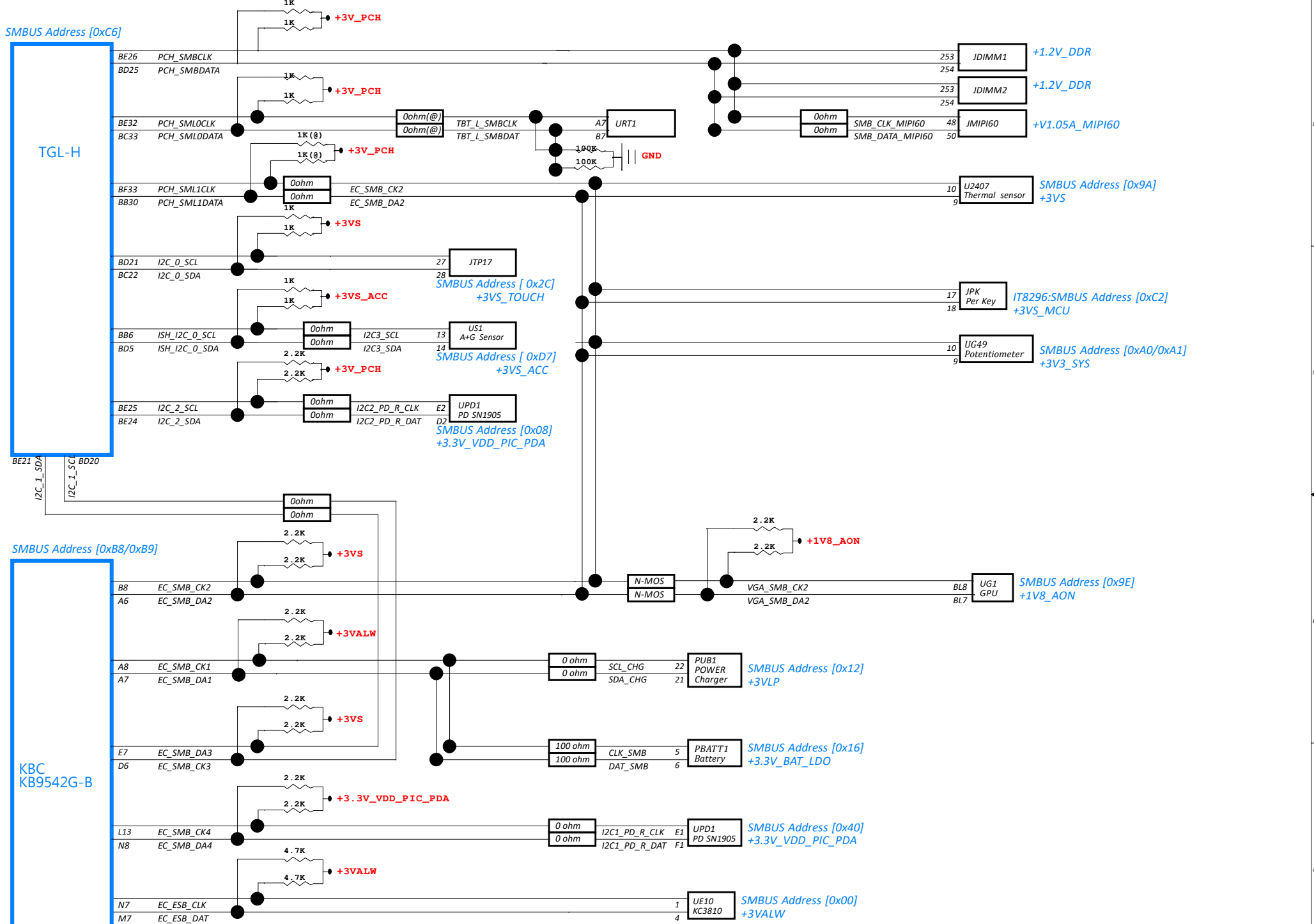
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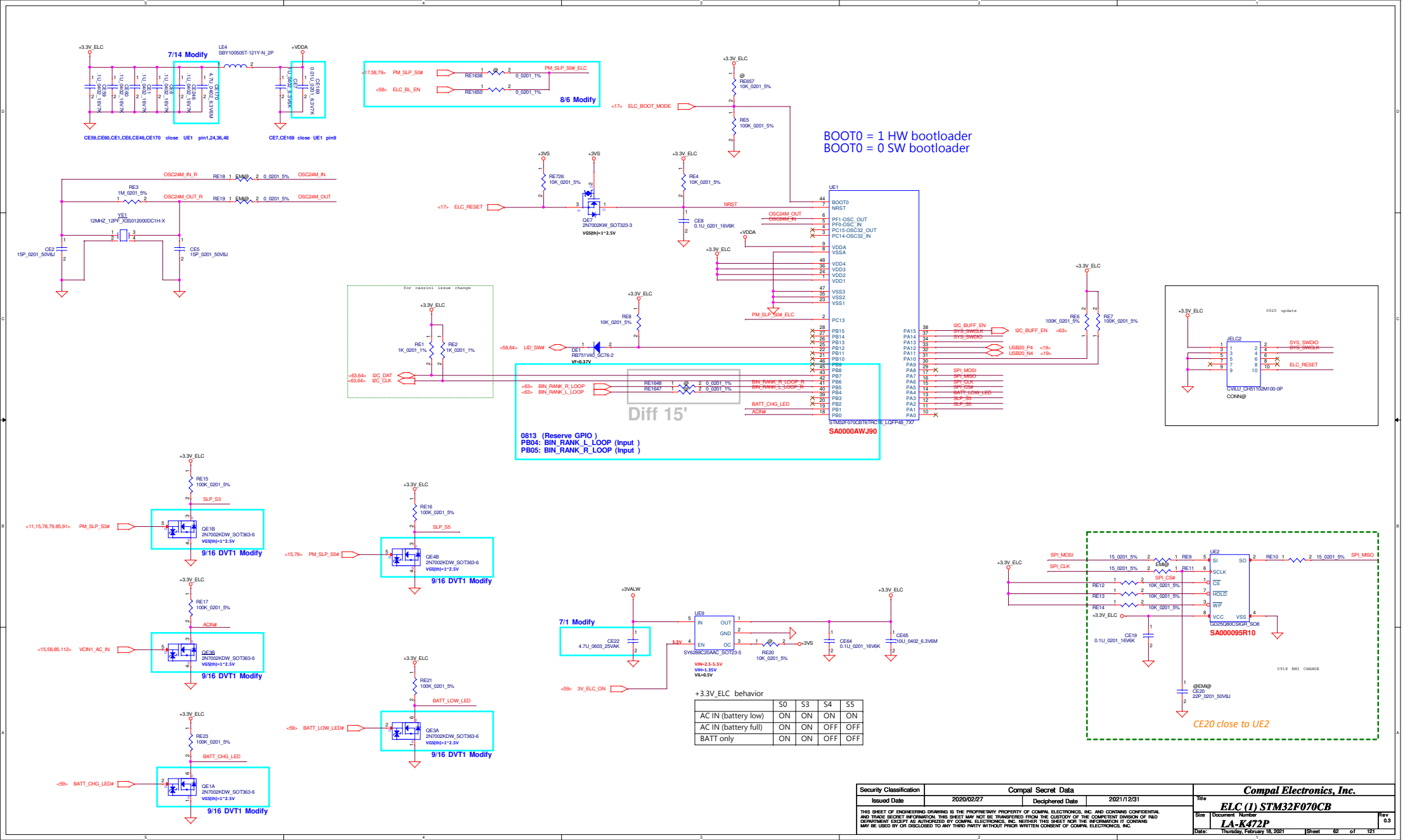
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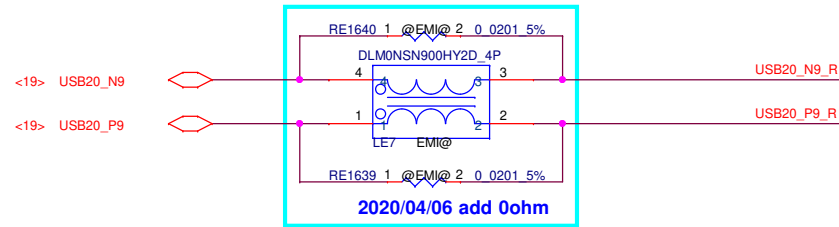
TGL-H

SMBUS Address [0xB8/0xB9]

KBC
KB9542G-B



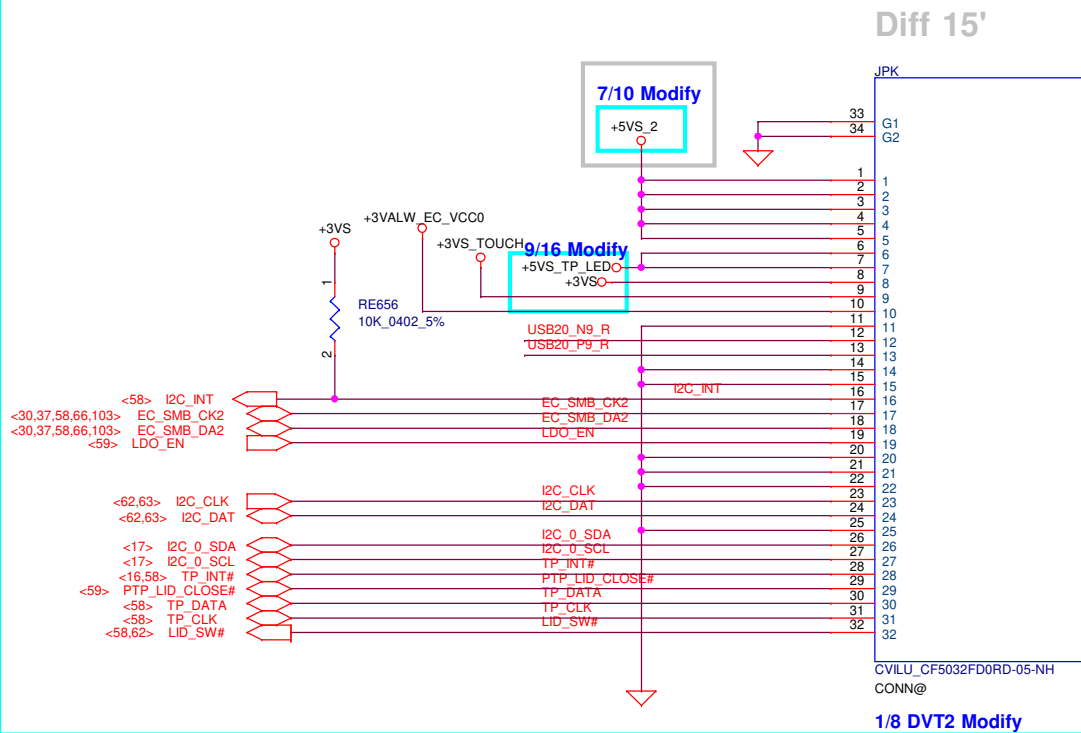




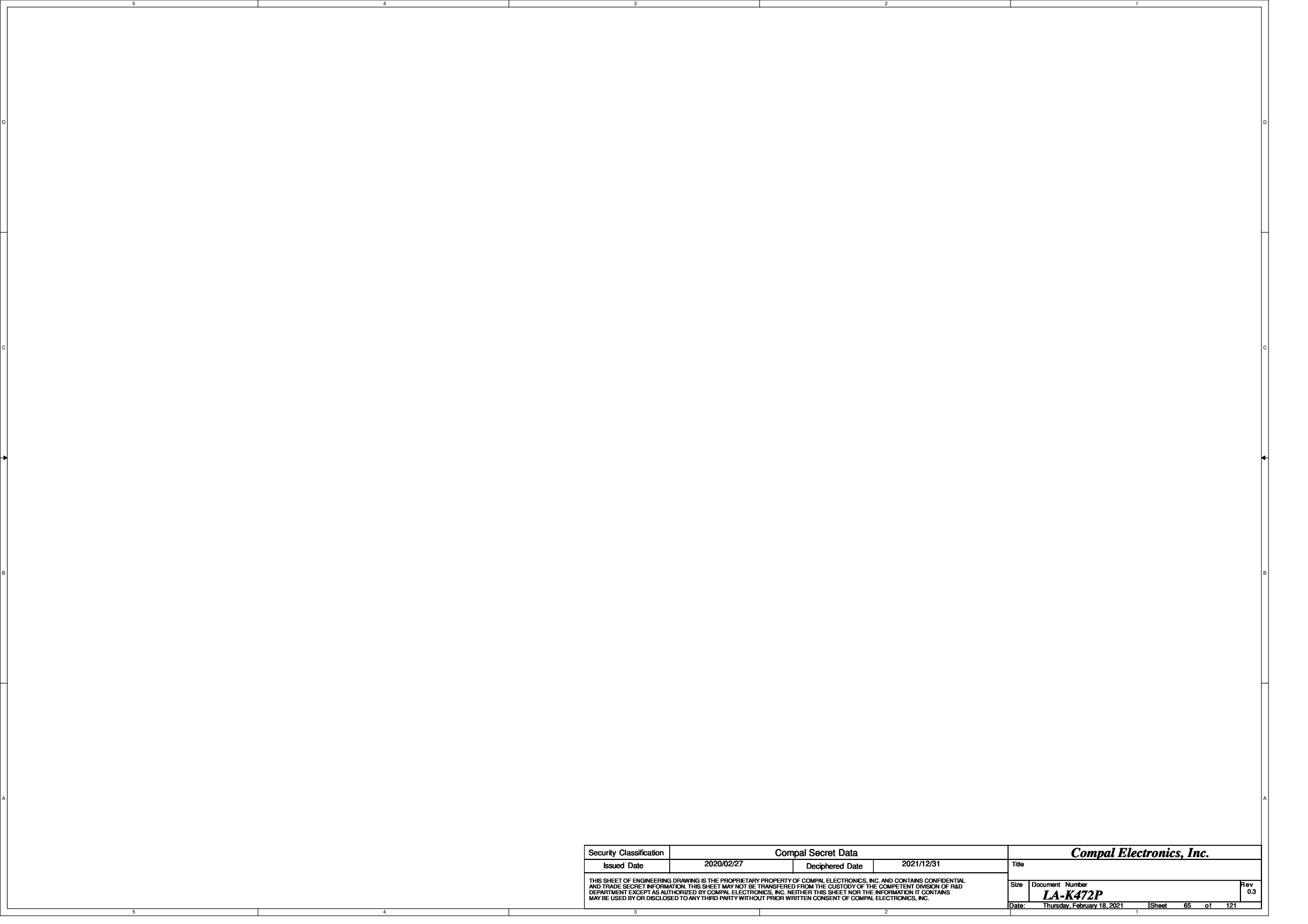
03/13 Change to 32pin (include TP/TP lighting/Hall sensor)

Per Key MCU board pin define

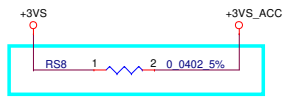
Pin1~5 +5VS
 Pin6~7 +5VS_TP_LED
 Pin8 +3VS
 Pin9 +3S_TOUCH
 Pin10 +3VALW_EC_VCC0
 Pin11 GND
 Pin12 D-
 Pin13 D+
 Pin14~15 GND
 Pin16 I2C_INT
 Pin17 I2C_CLK(EC)
 Pin18 I2C_DAT(EC)
 Pin19 LDO_EN
 Pin20~22 GND
 Pin23 I2C_CLK
 Pin24 I2C_DAT
 Pin25 GND
 Pin26 I2C_0_SDA_R
 Pin27 I2C_0_SCL_R
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 Pin29 PTP_LED_CLOSE#
 Pin30 TP_DATA
 Pin31 TP_CLK
 Pin32 LID_SW#



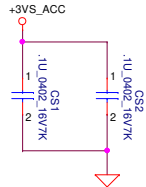
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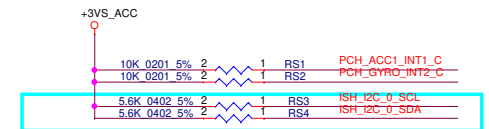
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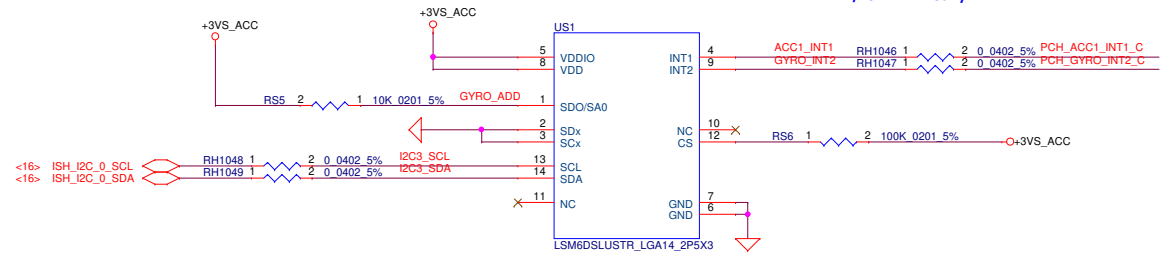
7/22 Modify



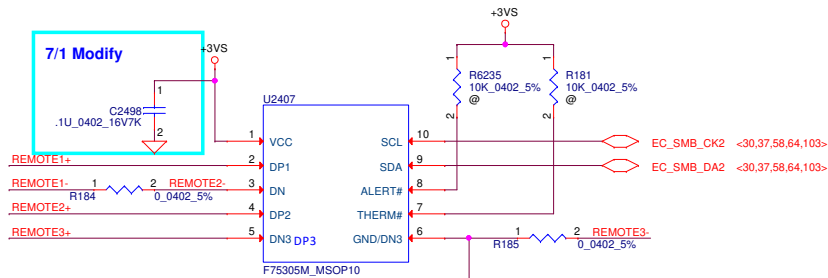
CS1,CS2 Close to US1



1/20 DVT2 Modify



Fintek thermal sensor---> CPU core, DIMM

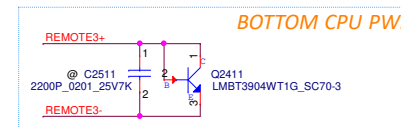
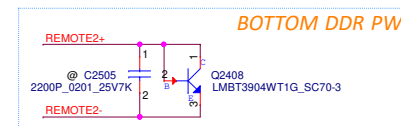
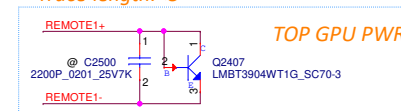


Address 1001_101xb

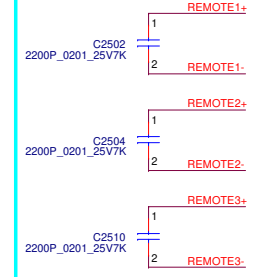
2nd source

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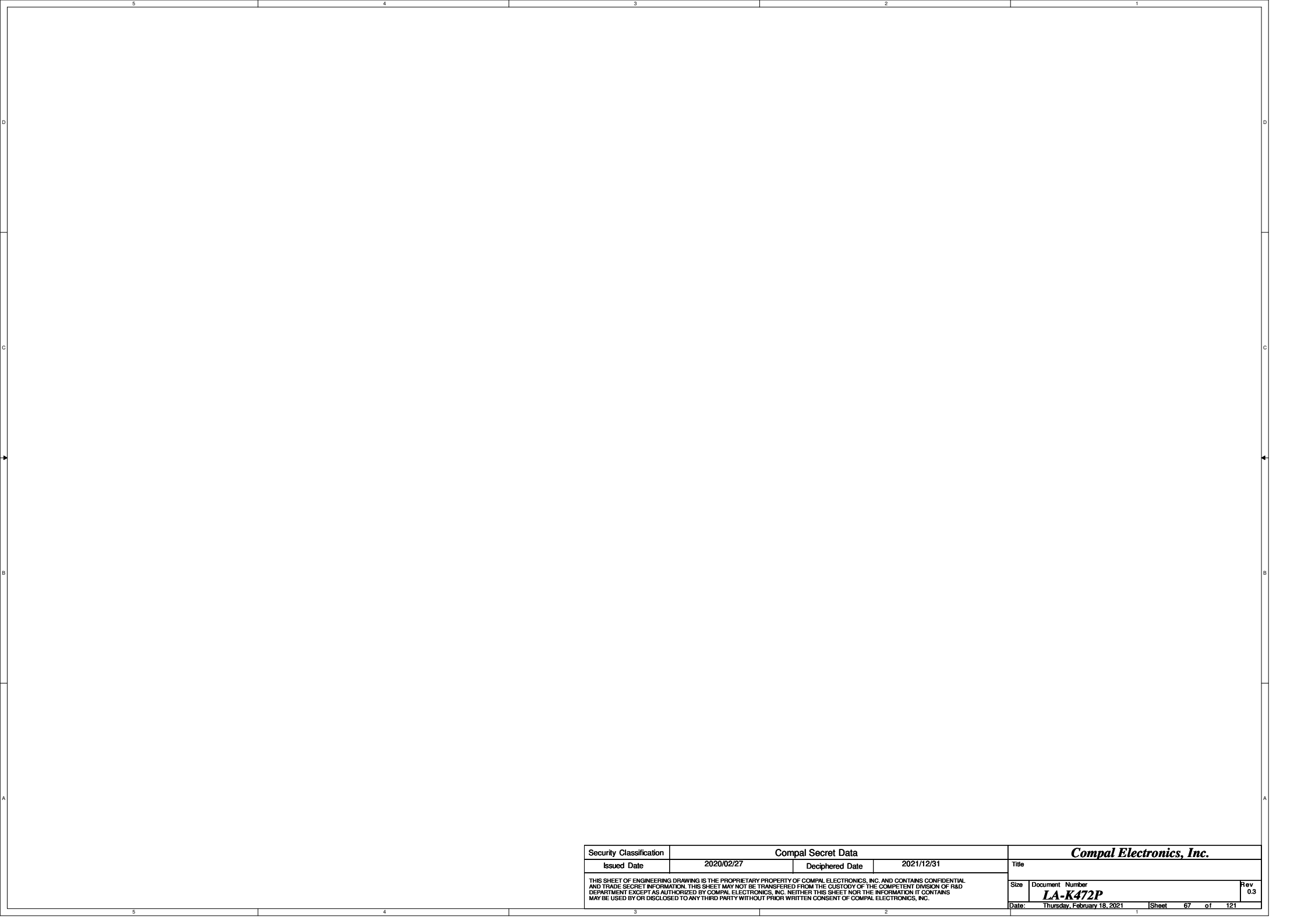
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Trace width/space:10/10 mil
Trace length:<8"



Close U2407

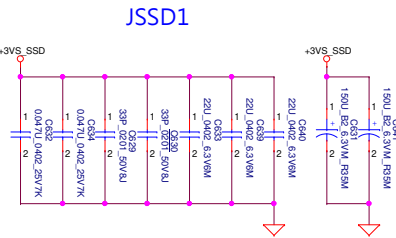
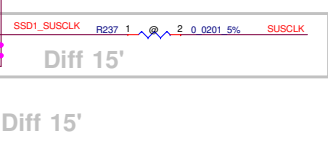
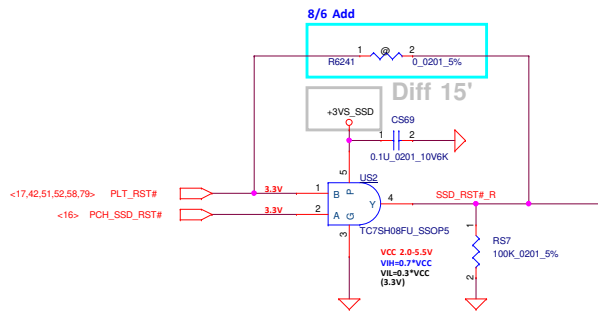
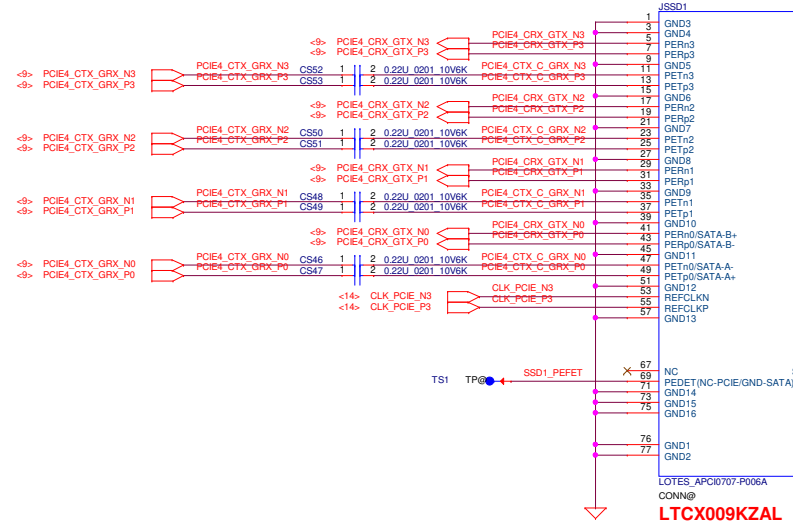


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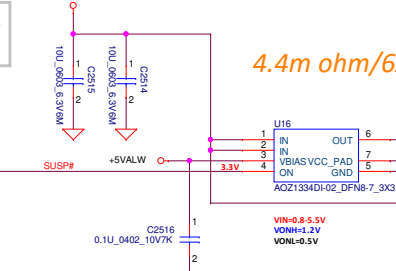
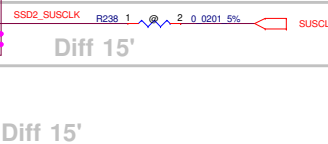
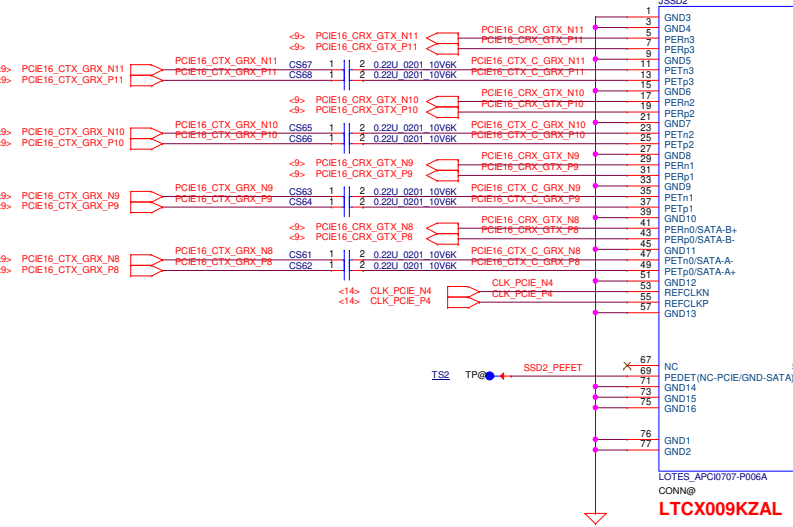


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PCIe Gen4 SSD#1, 2280



PCIe Gen4 SSD#2, 2280

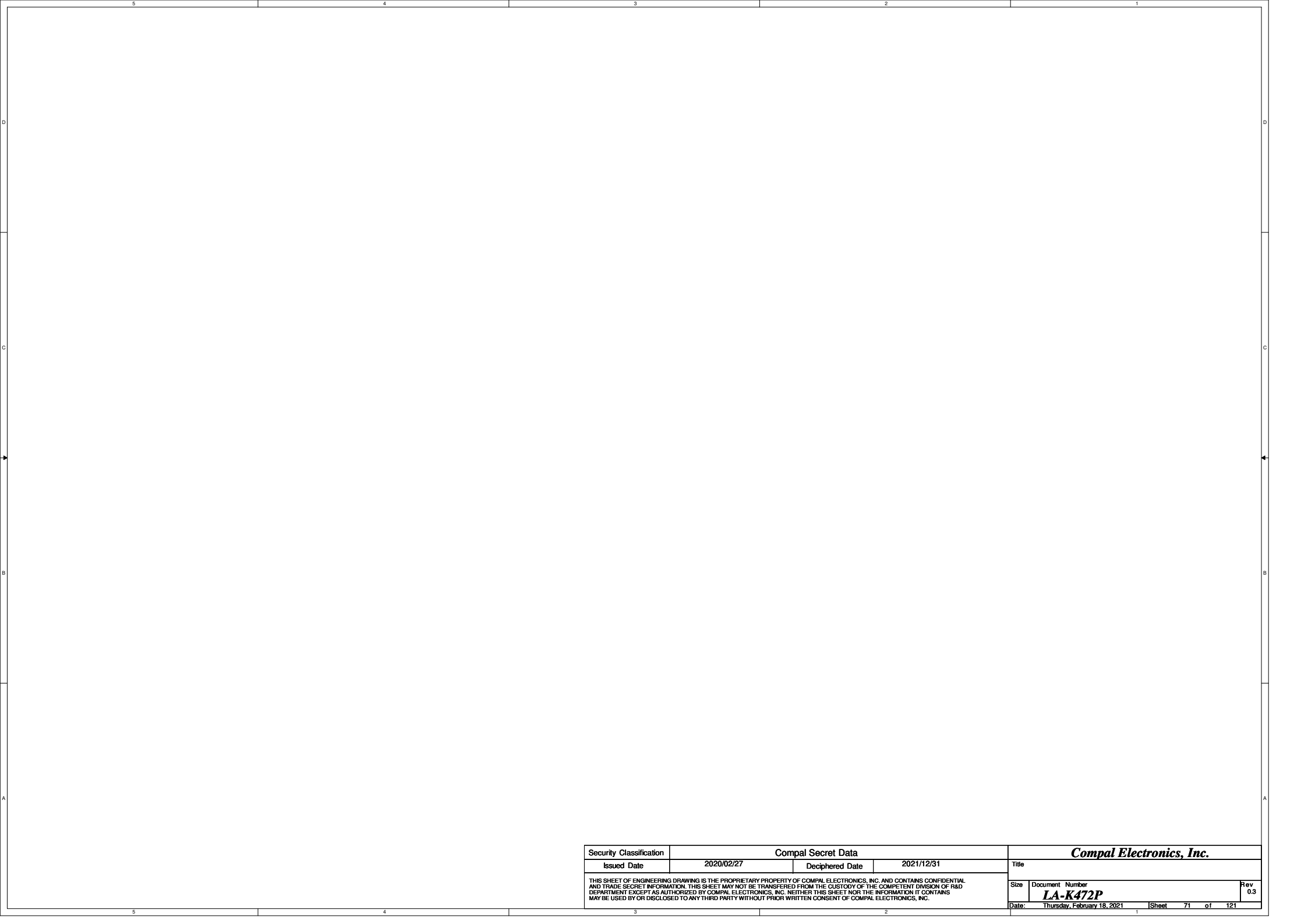


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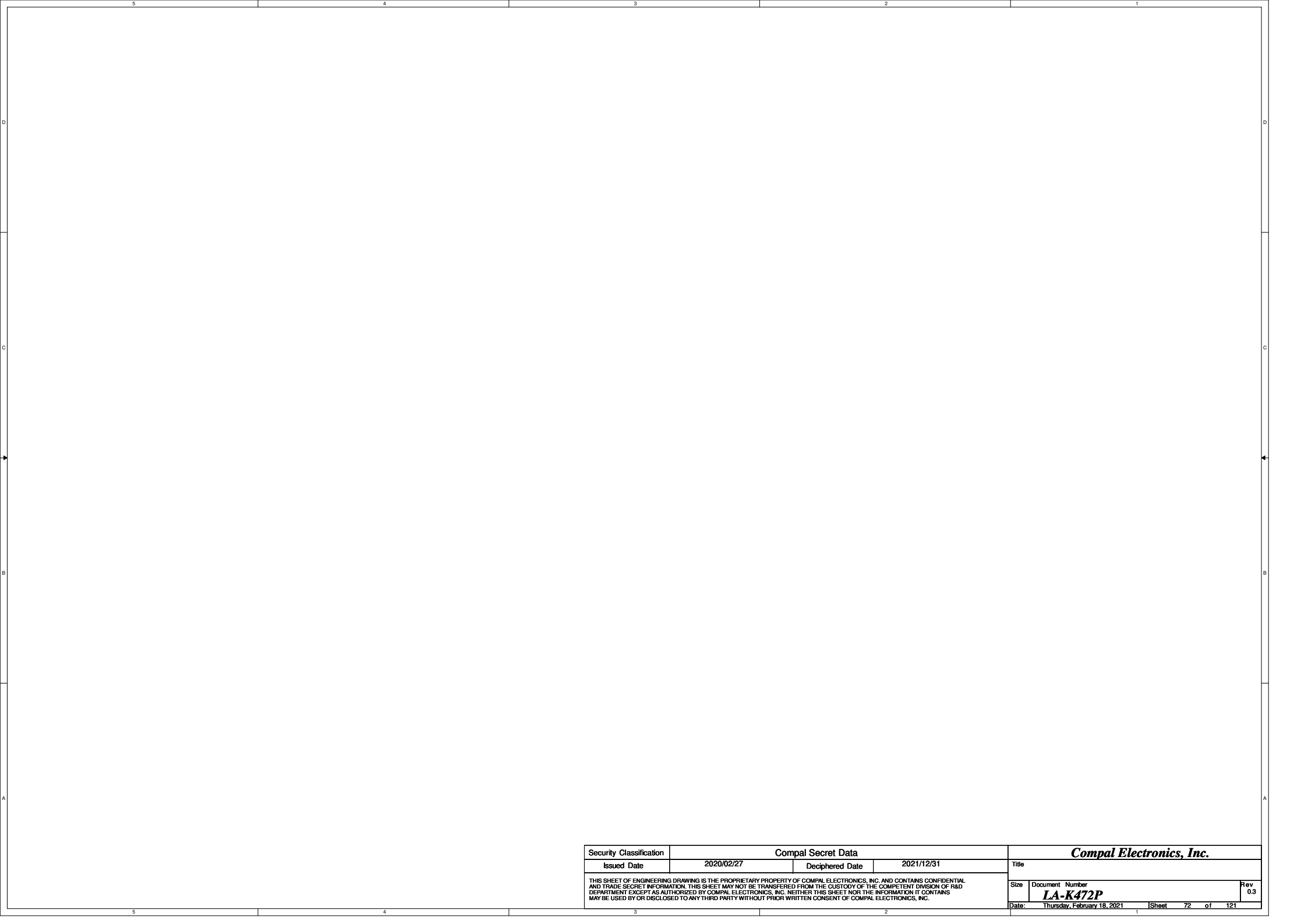
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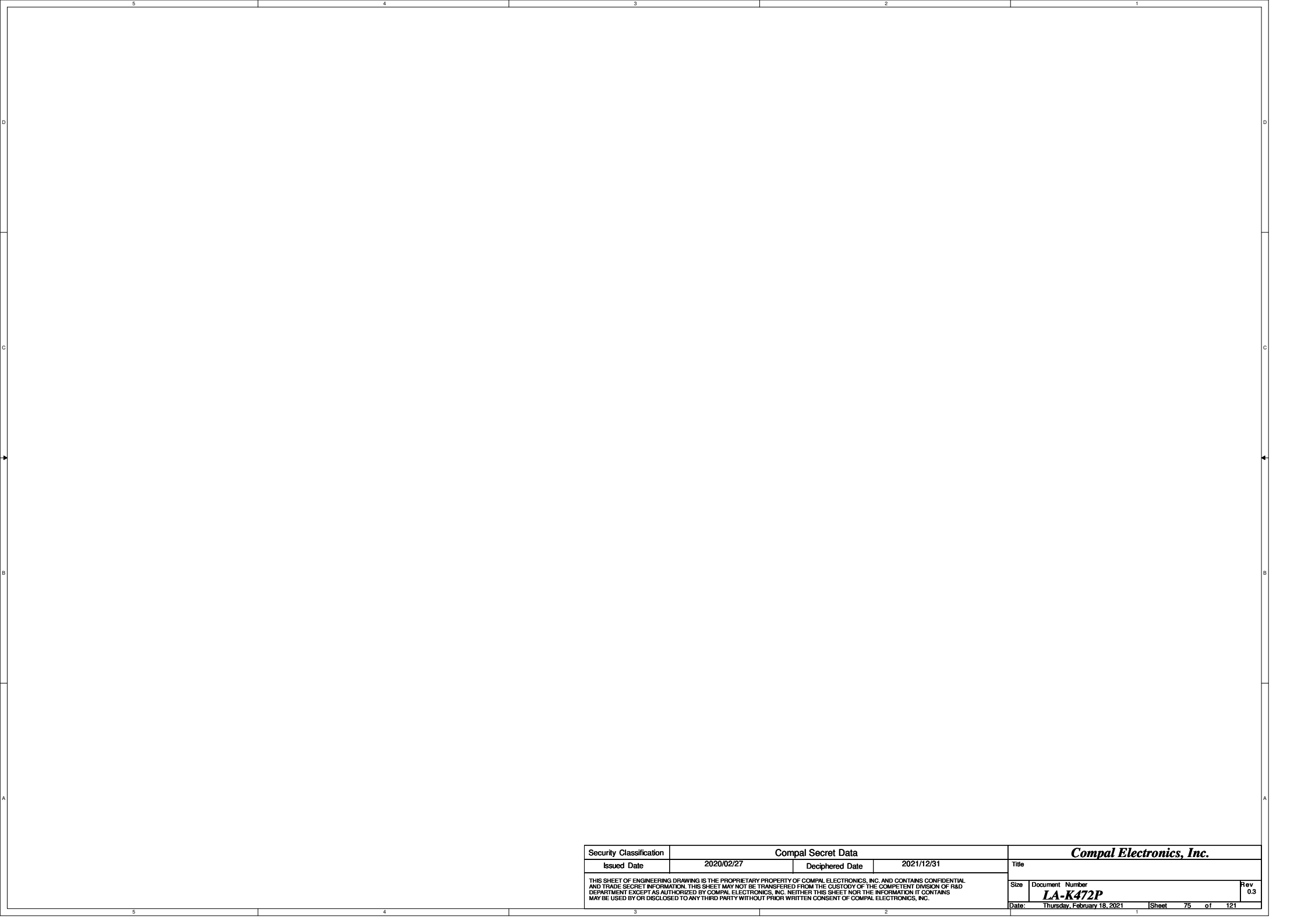


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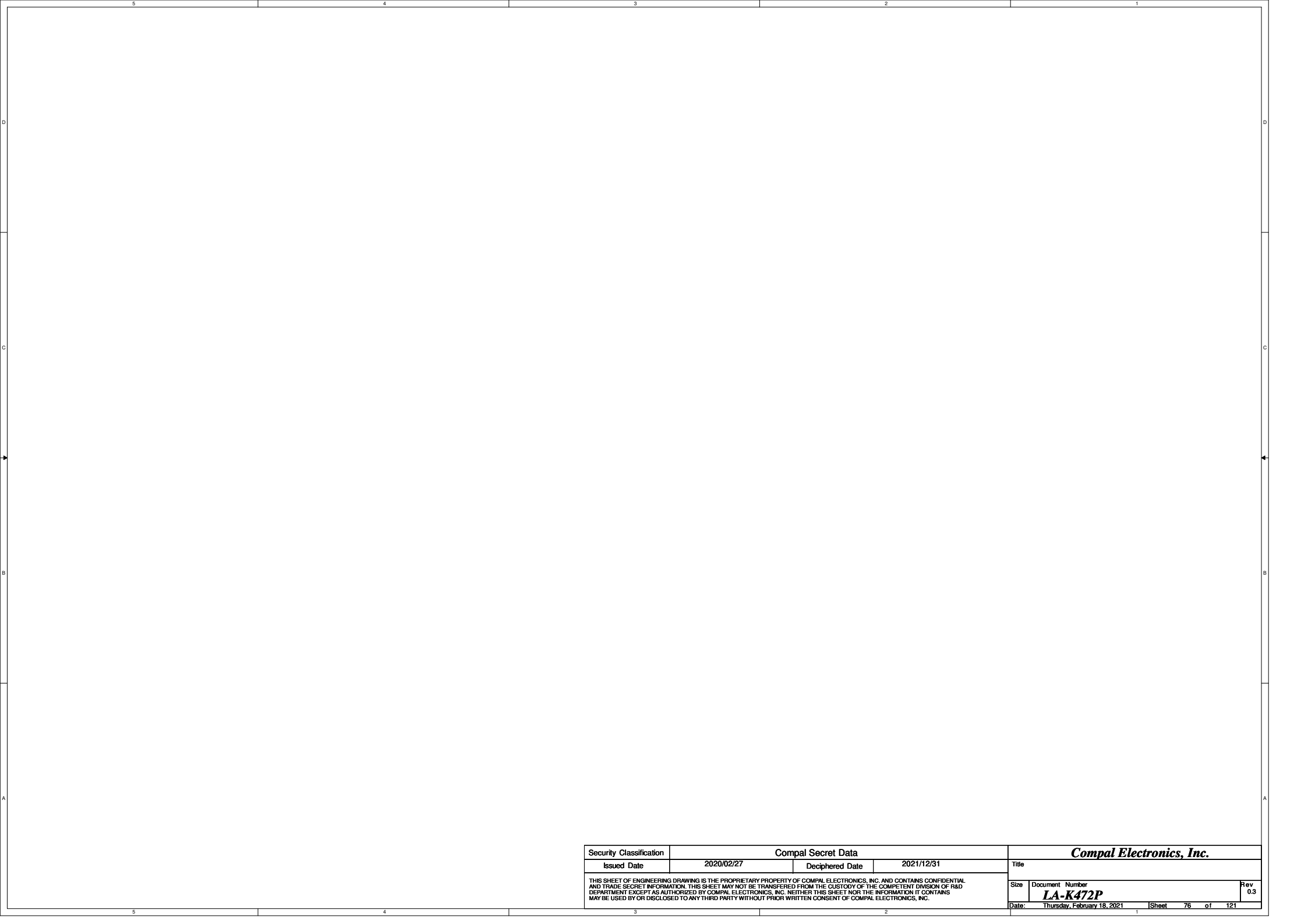


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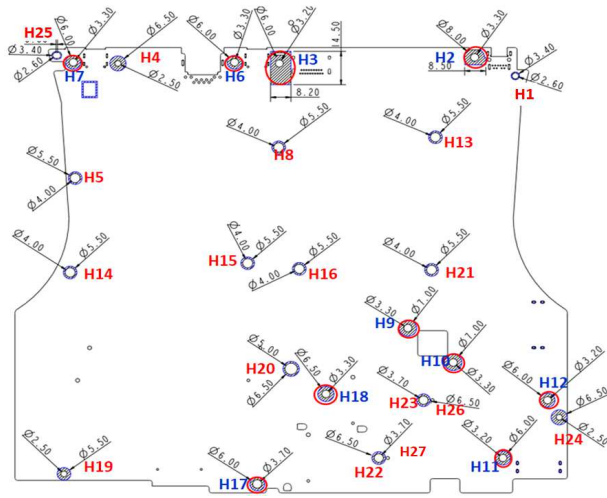
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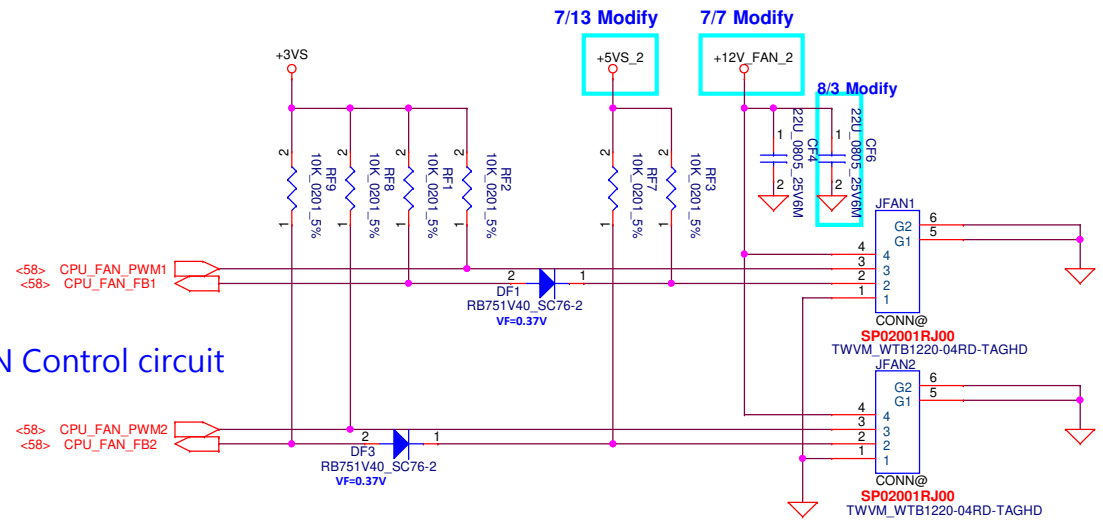
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Main Func = Screw

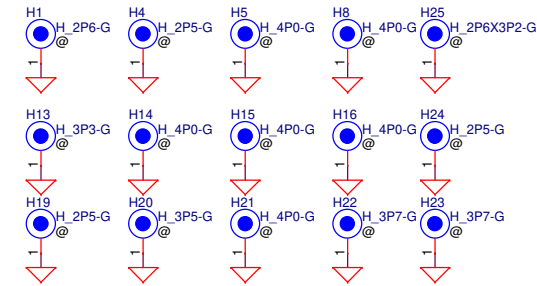
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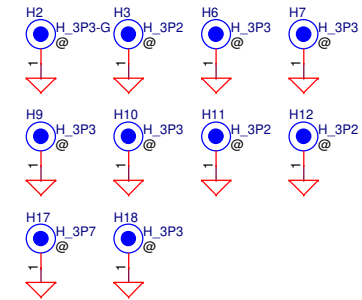
CPU FAN Control circuit



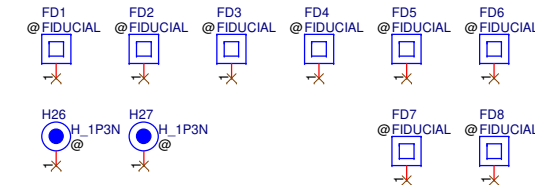
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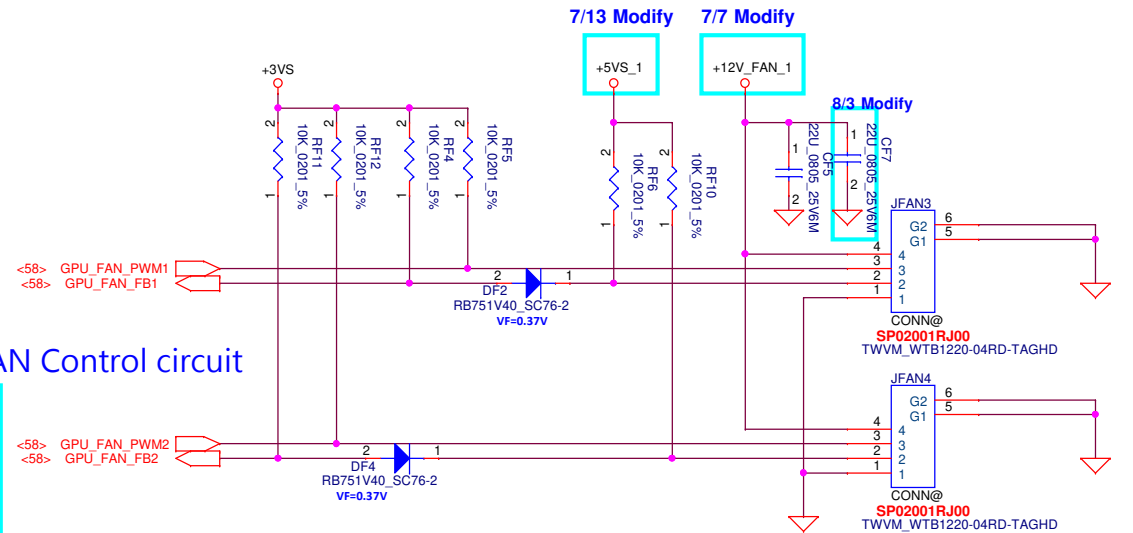
Stand-off



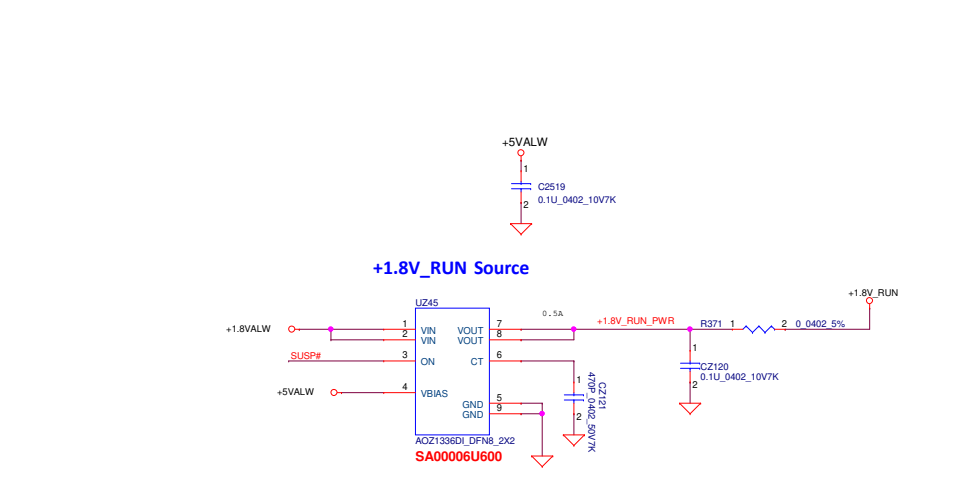
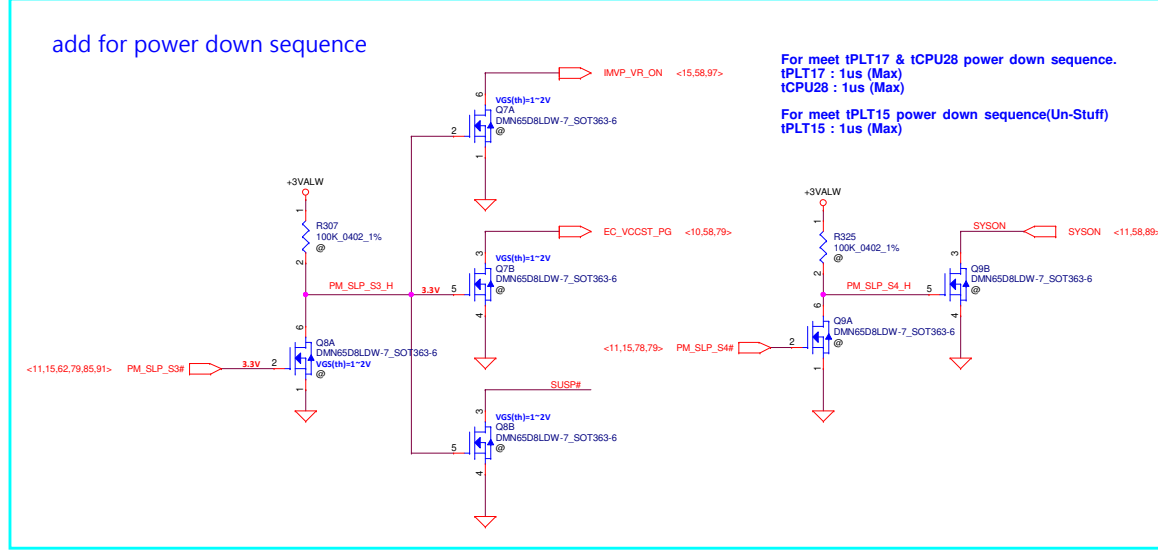
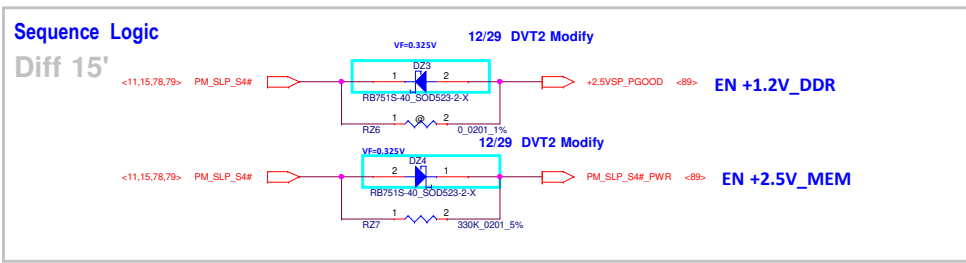
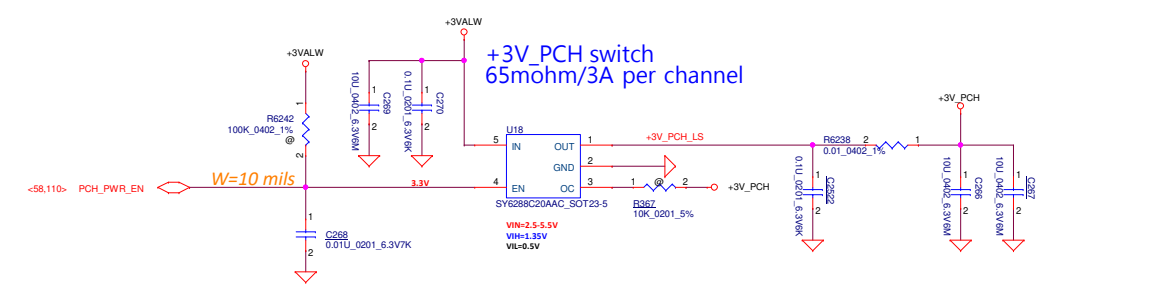
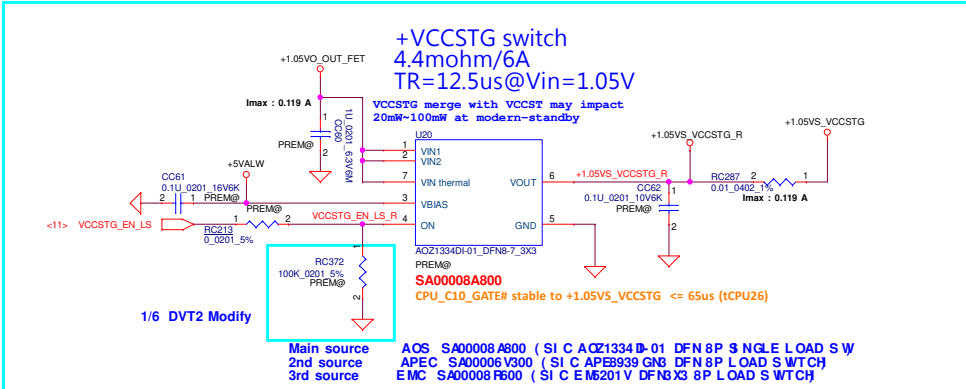
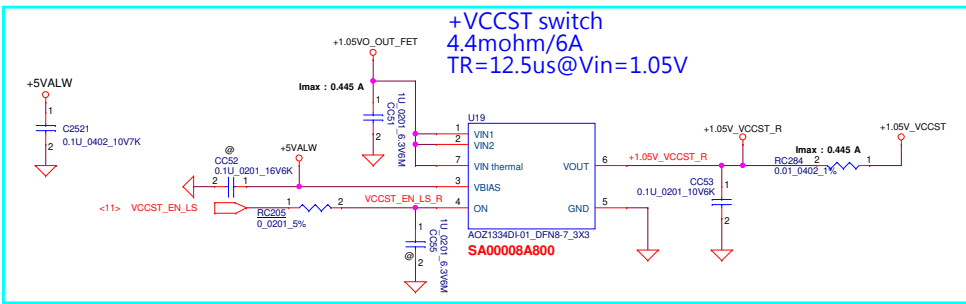
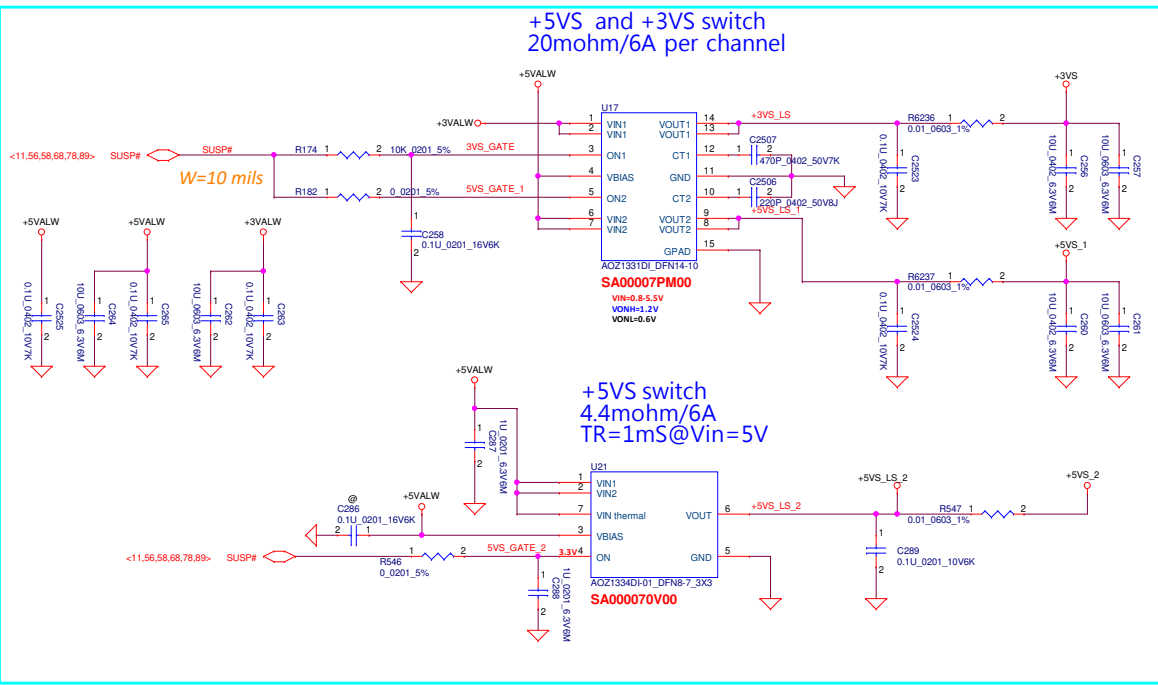
Fiducial Mark



GPU FAN Control circuit

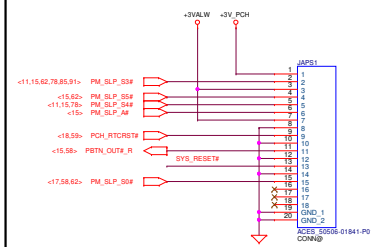
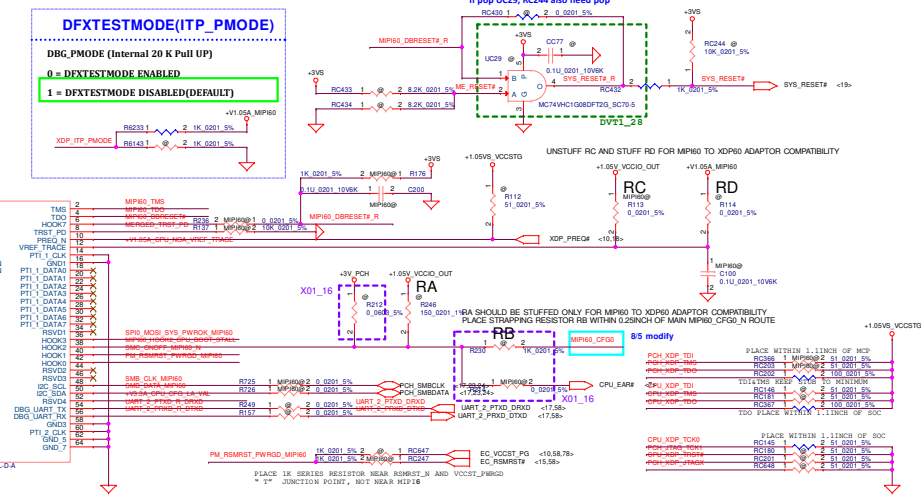
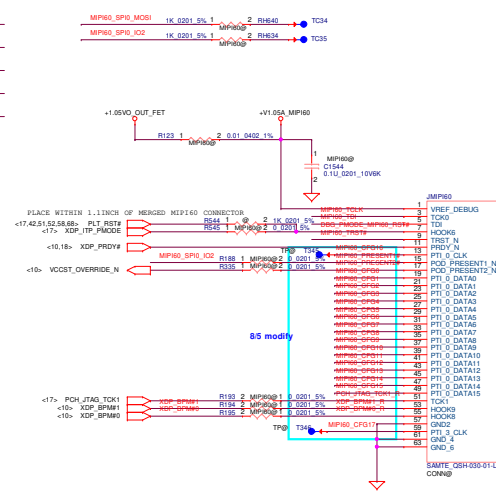
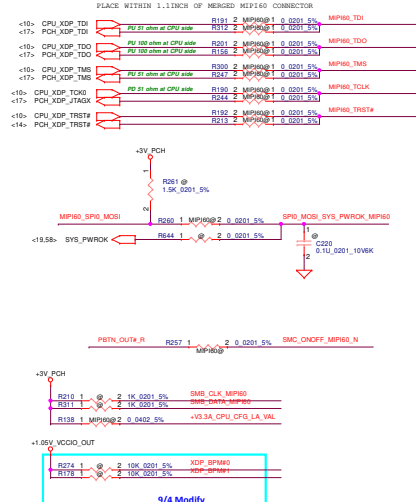


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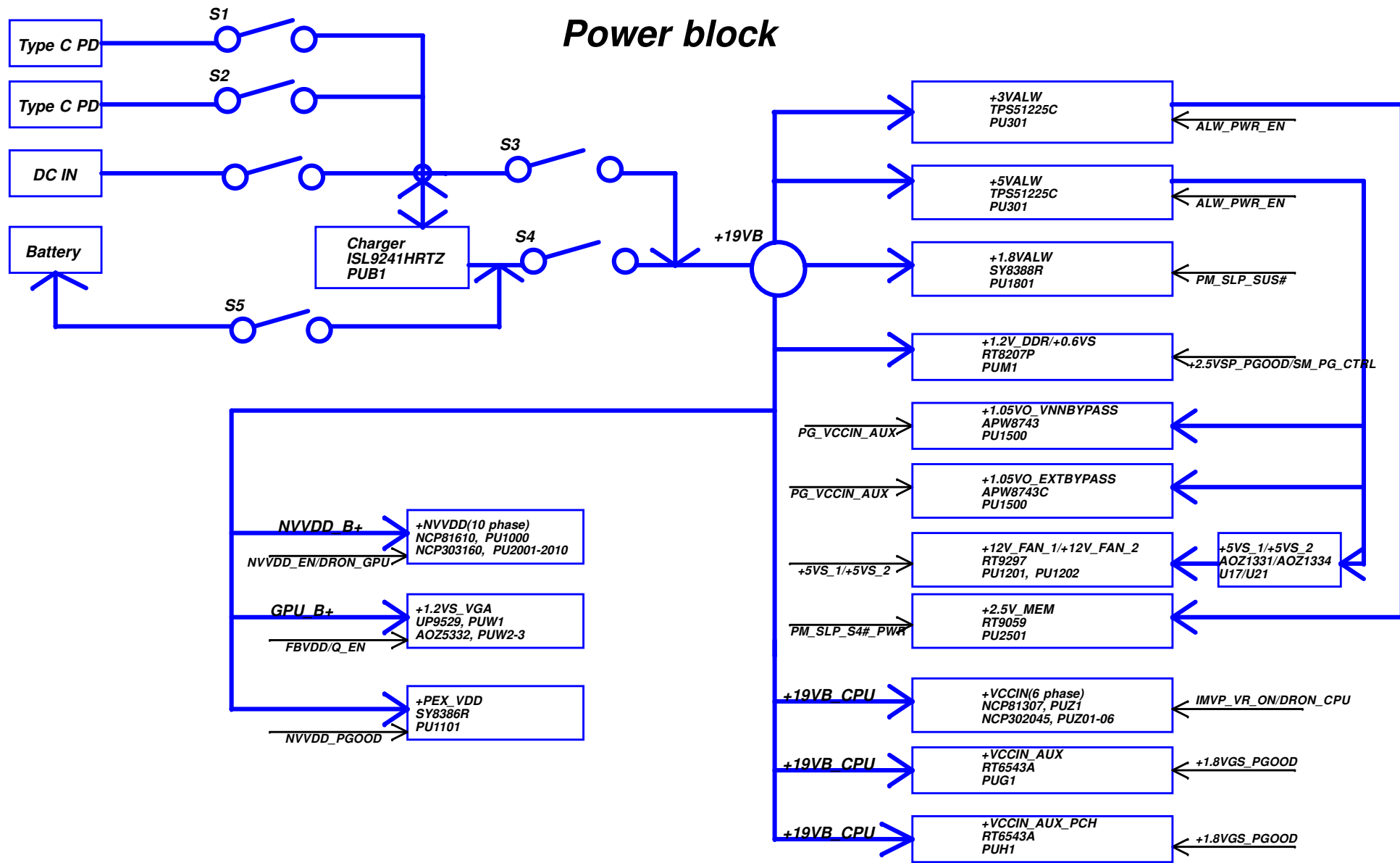


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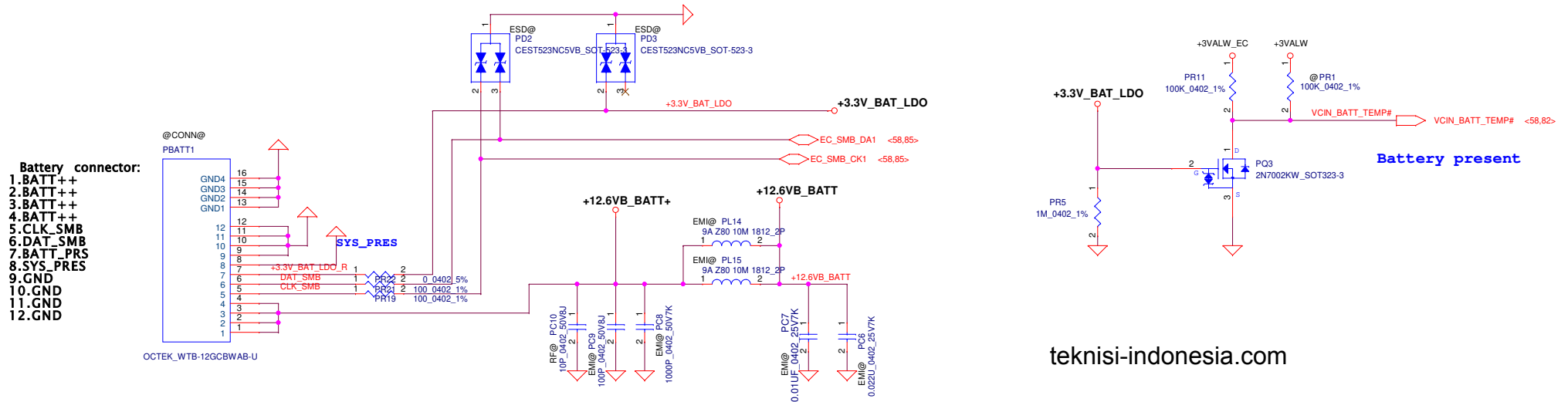
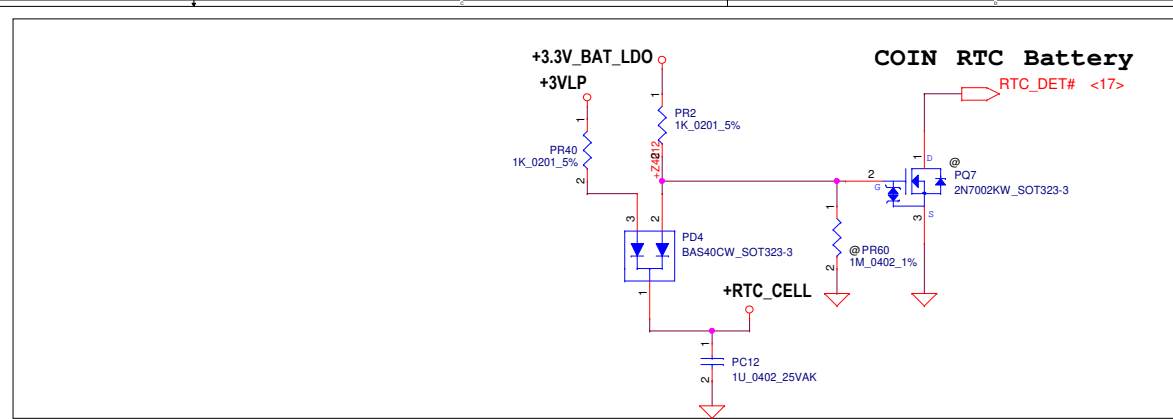
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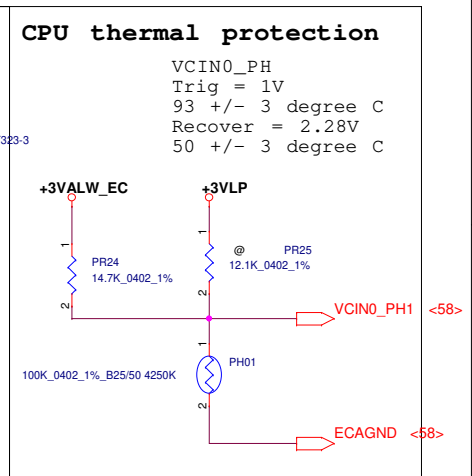
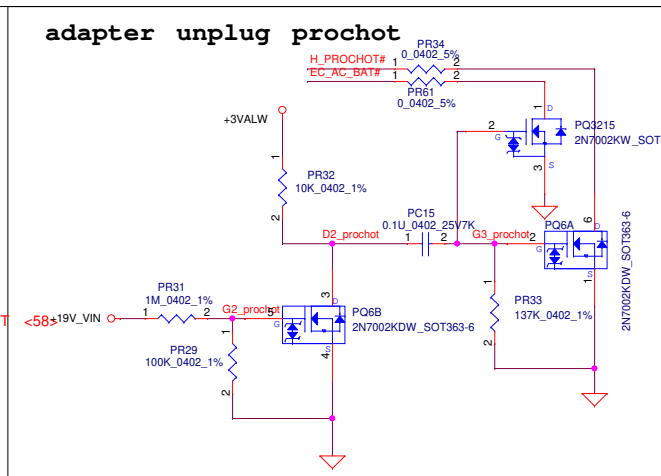
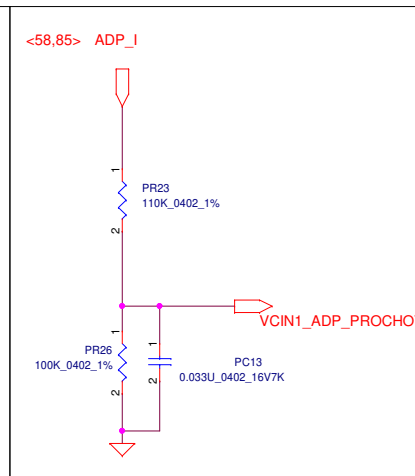
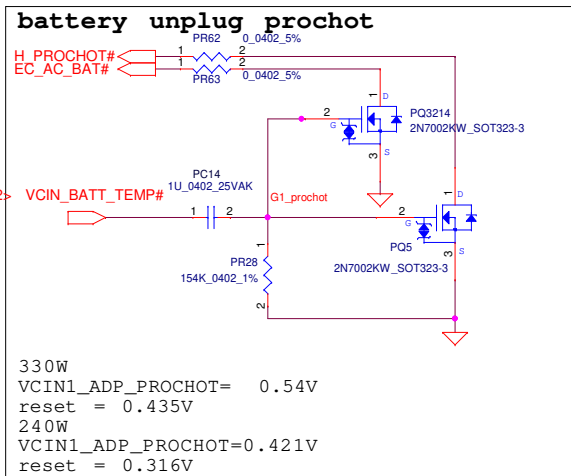
5	4	3	2	1																																			
D				D																																			
C				C																																			
B				B																																			
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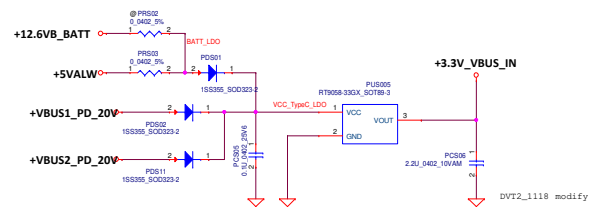
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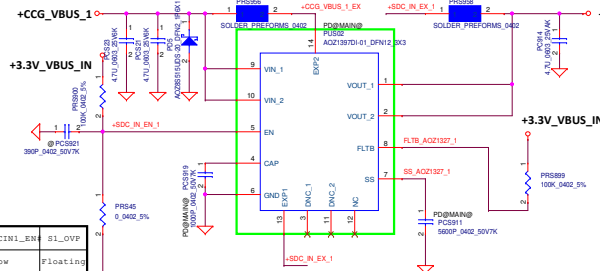
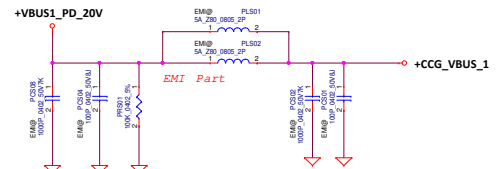


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Change to AOZ1397

Use AOZ1394 symbol and footprint for co-layout with NCP45766



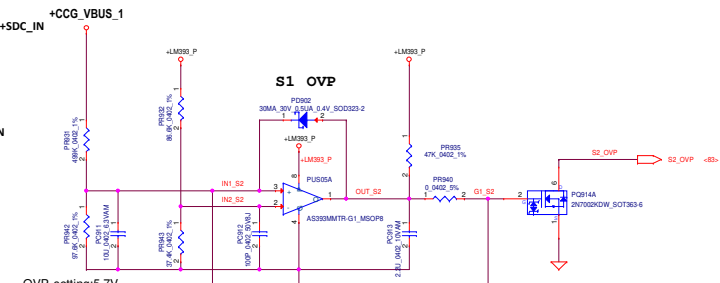
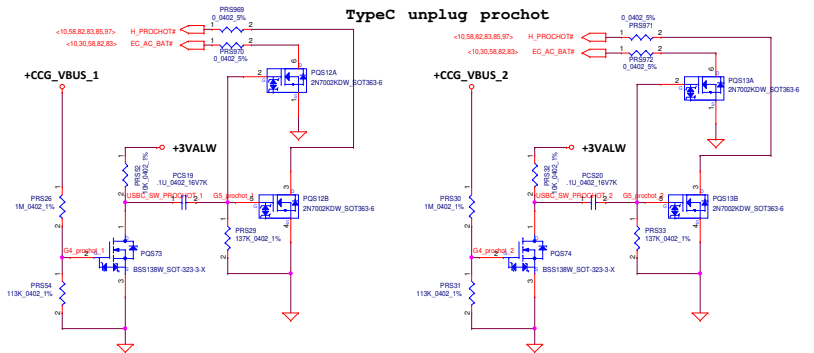
Type-C load switch signal state of EN pin

PDS02	PA_GATE_VSYS	OV_UV_P1EC_S1_SRP	TYPEC_DCIN1_EN	S1_OVP
Enable	High	Low	Low	Floating
Disable (either)	Low	High	High	Low

AOZ1397 EN pin Enable Active High. EN Pin Input High Threshold AOZ1397 is 1.4V, NCP45766 and NCP45767 is 1.5V

Type-C load switch source option

Source	Main	2nd	3rd
PDS02	AOZ1397	NCP45766	NCP45767
PC9911	5.6nF	NA	NA
PC9919	In	NA	NA
PC9956, 958	NA	0 ohm	0 ohm

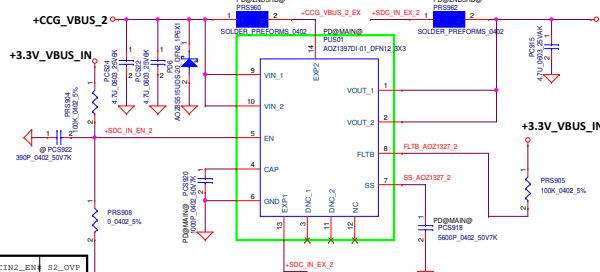
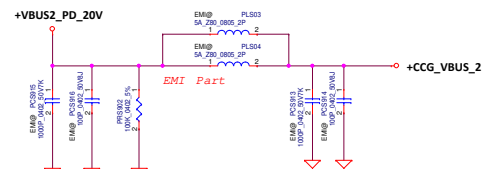


S1 OVP

OVP setting:5.7V

Change to AOZ1397

Use AOZ1394 symbol and footprint for co-layout with NCP45766



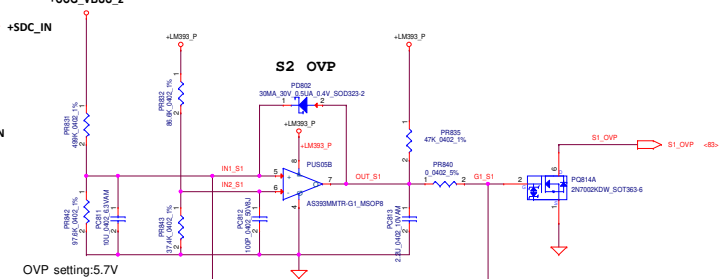
Type-C load switch signal state of EN pin

PDS01	PA_GATE_VSYS	OV_UV_P1EC_S1_SRP	TYPEC_DCIN2_EN	S2_OVP
Enable	High	Low	Low	Floating
Disable (either)	Low	High	High	Low

AOZ1397 EN pin Enable Active High. EN Pin Input High Threshold AOZ1397 is 1.4V, NCP45766 and NCP45767 is 1.5V

Type-C load switch source option

Source	Main	2nd	3rd
PDS01	AOZ1397	NCP45766	NCP45767
PC9918	5.6nF	NA	NA
PC9920	In	NA	NA
PC9960, 962	NA	0 ohm	0 ohm



S2 OVP

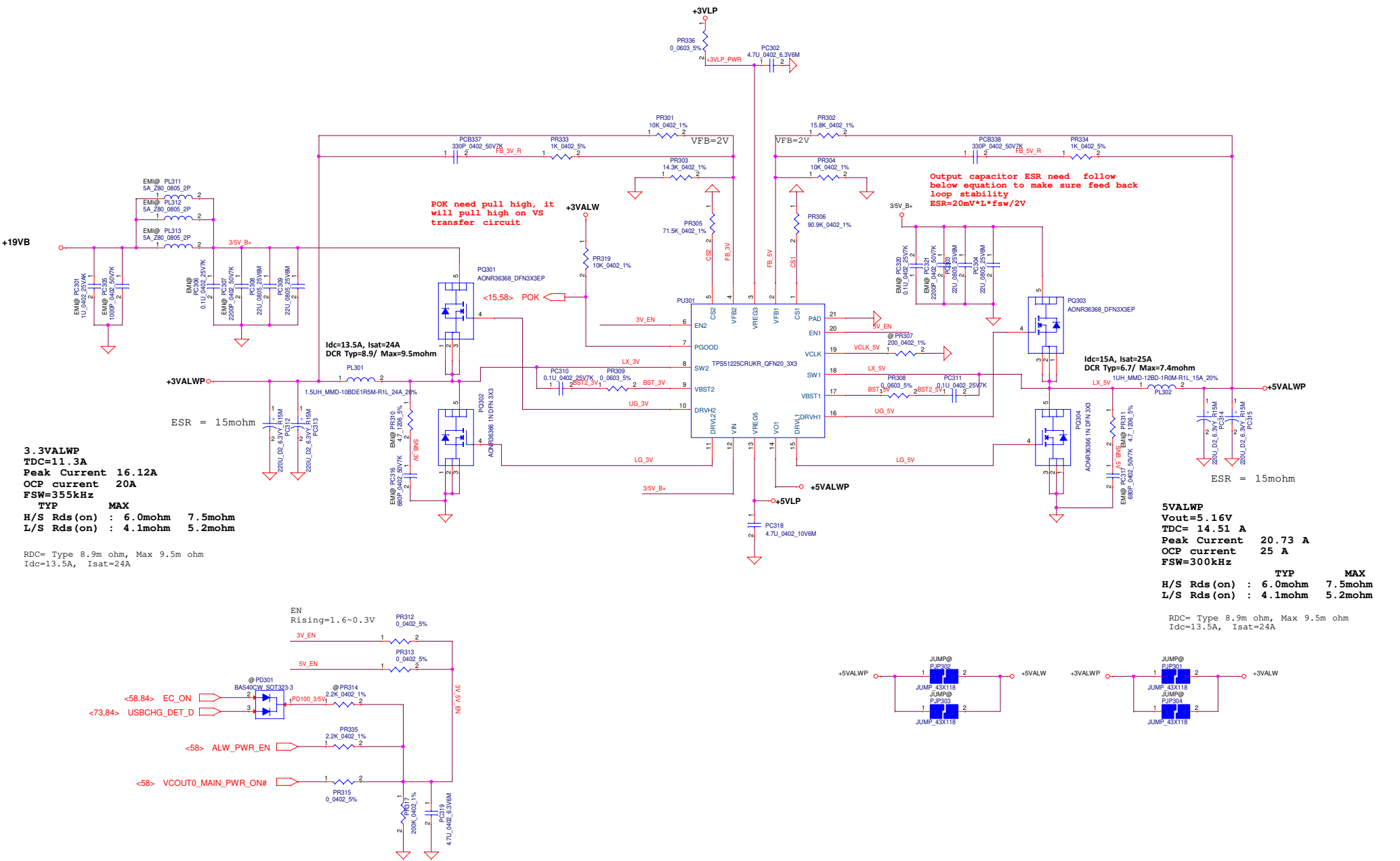
OVP setting:5.7V

[illegible]

S5

Reserve

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3.3VALWP
TDC=11.3A
Peak Current 16.12A
OCP current 20A
FSW=355kHz

	TYP	MAX
H/S Rds(on)	6.0mohm	7.5mohm
L/S Rds(on)	4.1mohm	5.2mohm

RDC= Type 8.9m ohm, Max 9.5m ohm
Idc=13.5A, Isat=24A

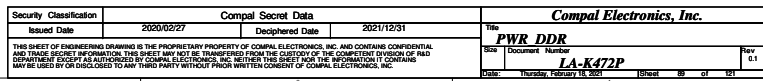
5VALWP
Vout=5.16V
TDC= 14.51 A
Peak Current 20.73 A
OCP current 25 A
FSW=300kHz

	TYP	MAX
H/S Rds(on)	6.0mohm	7.5mohm
L/S Rds(on)	4.1mohm	5.2mohm

RDC= Type 8.9m ohm, Max 9.5m ohm
Idc=13.5A, Isat=24A

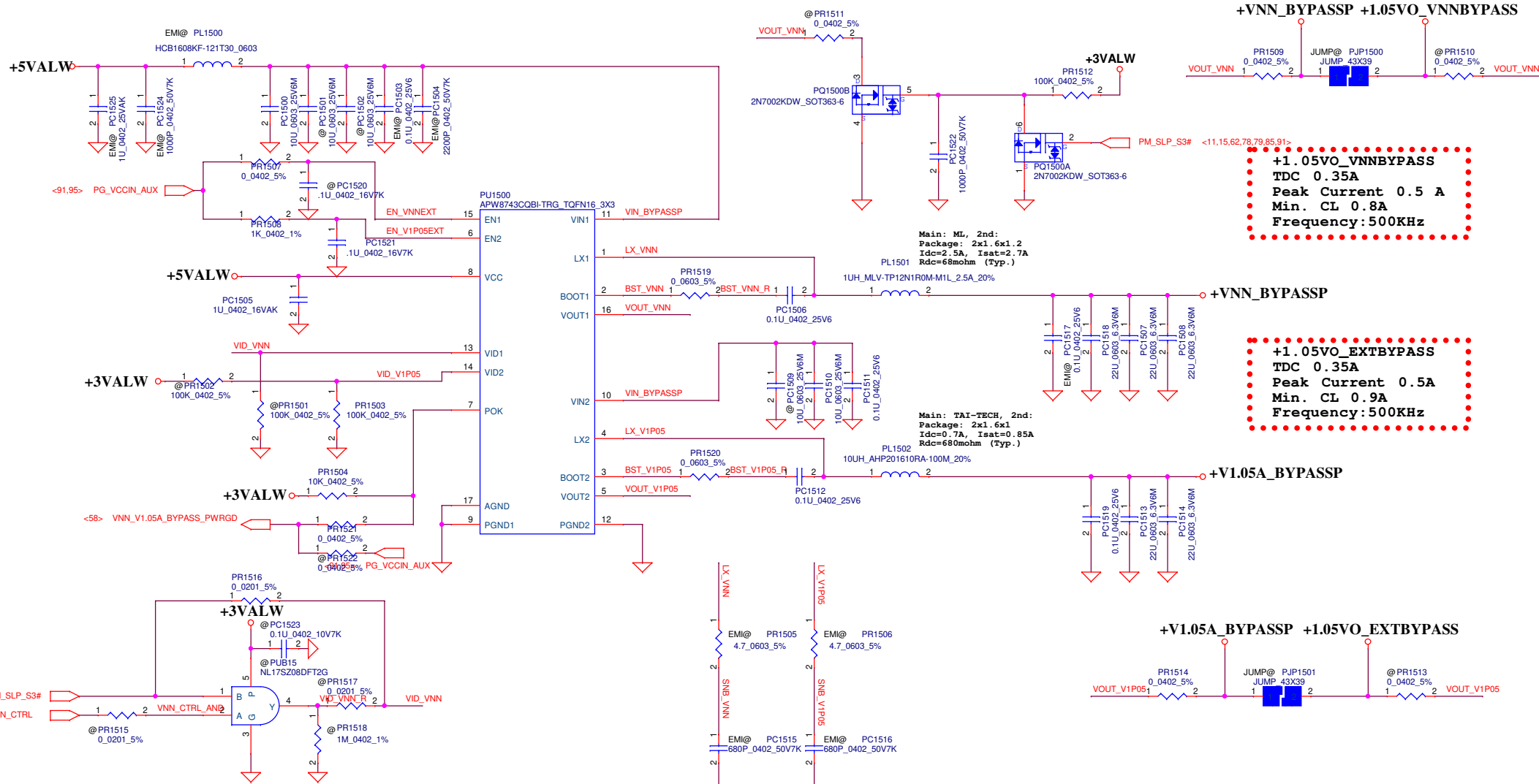
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+1.05VO_VNNBYPASS
TDC 0.35A
Peak Current 0.5 A
Min. CL 0.8A
Frequency: 500KHz

+1.05VO_EXTBYPASS
TDC 0.35A
Peak Current 0.5A
Min. CL 0.9A
Frequency: 500KHz

+V1.05A_BYPASS +1.05VO_EXTBYPASS

Part Number	VID=0(VNN)	VID=1(VNN)	VID=0(V1P05A)	VID=1(V1P05A)
APW8743CQBI(QBGI)	1.05V	0.78V	1.05V	0.96V
APW8743DQBI(QBGI)	0.78V	0.7V	1.05V	0.96V
APW8743EQBI(QBGI)	1.05V	0.7V	1.05V	0.96V

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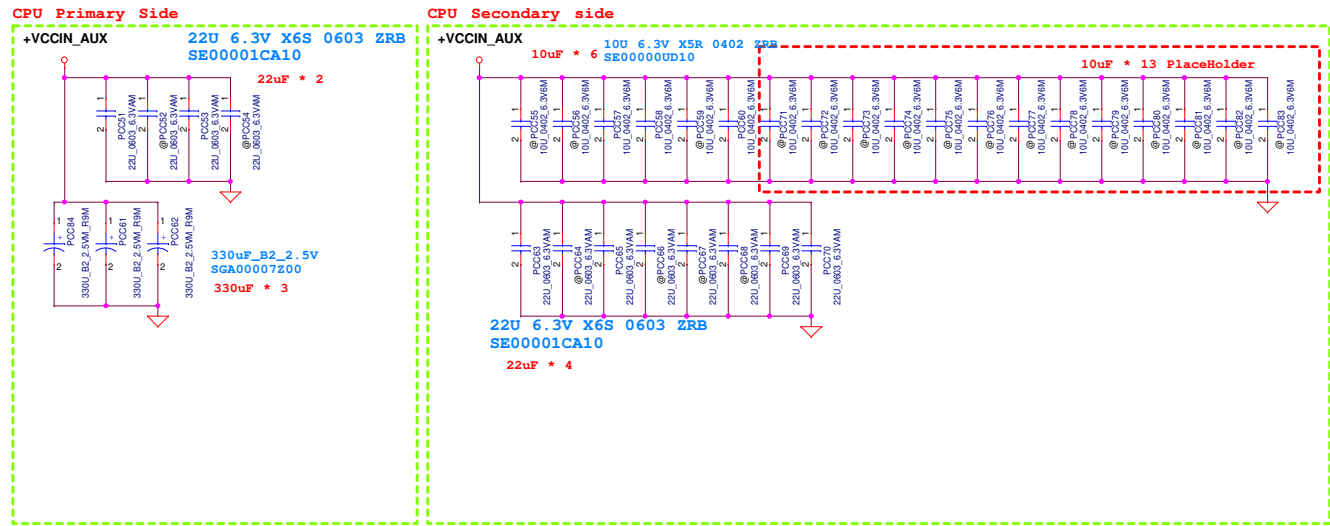
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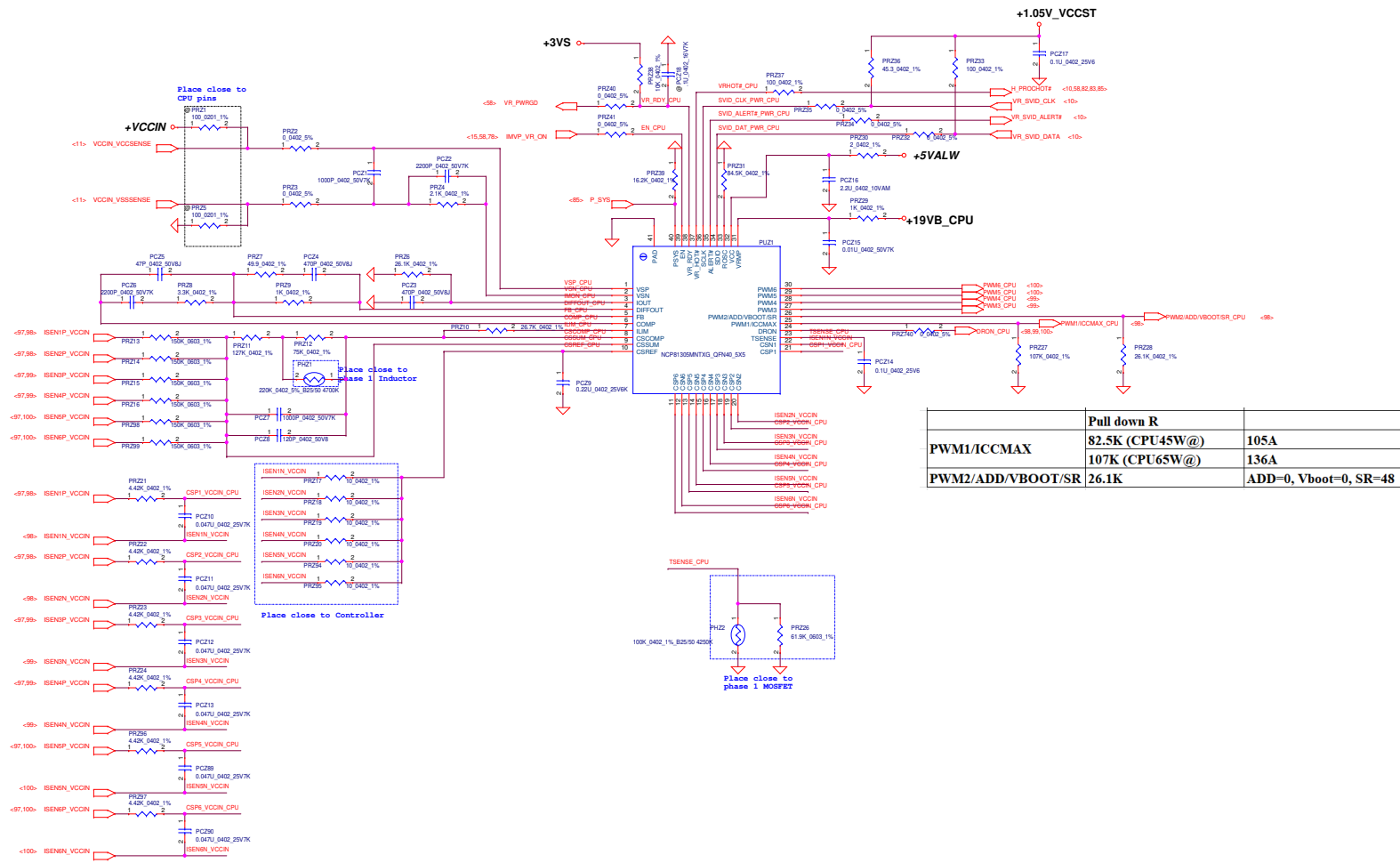
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+VCCIN_AUX Decoupling Cap



PDG Rev0p5
CPU65W
ICCMAX= 136A
TDC=102A (PL2)
OCP=177A
DC LL= 1.5 mohm
Fsw= 600kHz

PDG Rev1p0
CPU45W
ICCMAX= 105A
TDC=61A (PL2)
OCP=137A
DC LL= 1.5 mohm
Fsw= 600kHz

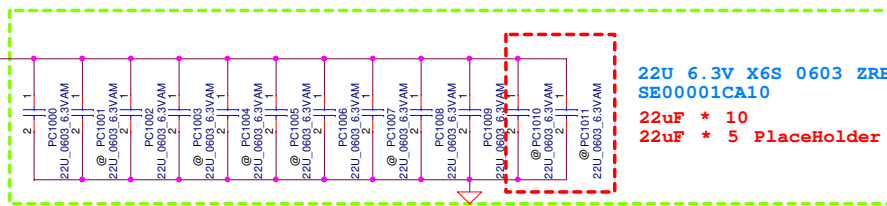


	Pull down R	
PWM1/ICCMAX	82.5K (CPU45W@)	105A
PWM2/ADD/VBOOT/SR	107K (CPU65W@)	136A
		ADD=0, Vboot=0, SR=48

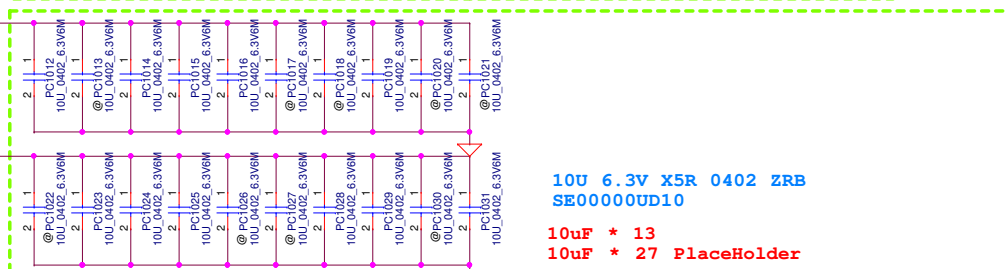
Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2020/02/27	Disseminated Date 2021/12/31
Document Number	PWR-IMVP9-NCP81307	
Date	Thursday, February 18, 2021	12:01:01

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2020/02/27	Deciphered Date	2021/12/31	Title	PWR +VCC CORE SW1&2	
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				Date:	Thursday, February 18, 2021	Sheet

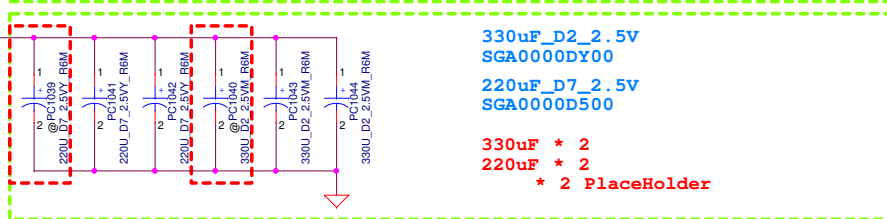
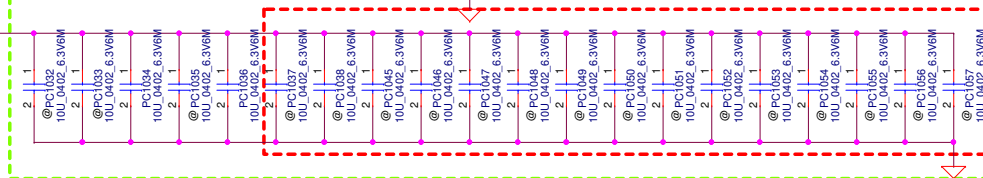
+VCCIN



22U 6.3V X6S 0603 ZRB
SE00001CA10
22uF * 10
22uF * 5 Placeholder



10U 6.3V X5R 0402 ZRB
SE00000UD10
10uF * 13
10uF * 27 Placeholder



330uF_D2_2.5V
SGA0000DY00
220uF_D7_2.5V
SGA0000D500
330uF * 2
220uF * 2
* 2 Placeholder

Intel PDG Rev0.8 excel
+VCCIN Output CAP :
47uF_0603 *10 pcs + reserved *2pcs
10uF_0402 *25 pcs + reserved *2pcs
220uF_D7 *4pcs + reserved *2pcs

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				Size	Document Number
				Date	Thursday, February 18, 2021
				Sheet	101 of 121
				Rev	0.1

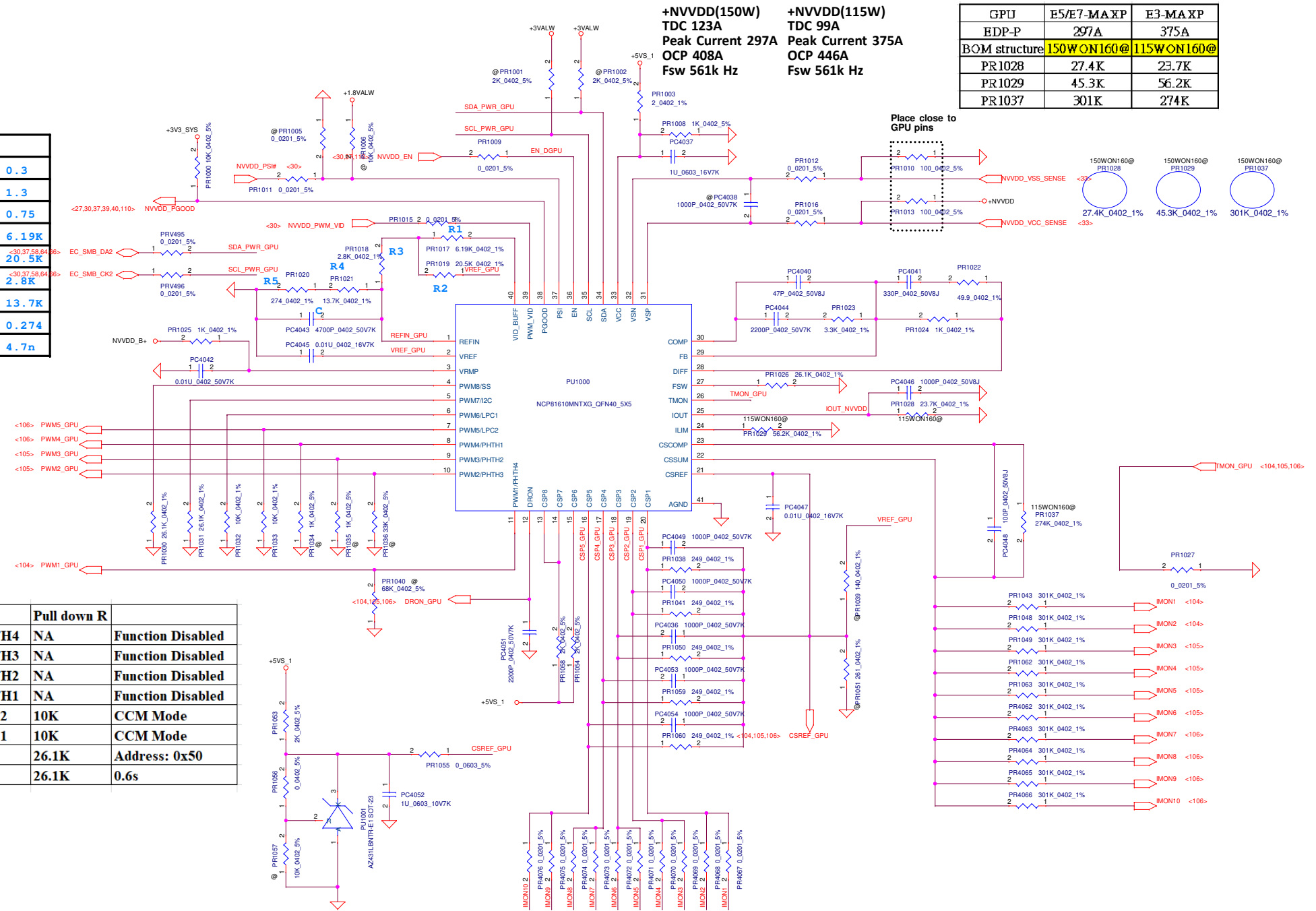
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					LA-K472P	0.1
				Date:	Thursday, February 18, 2021	Sheet 102 of 121

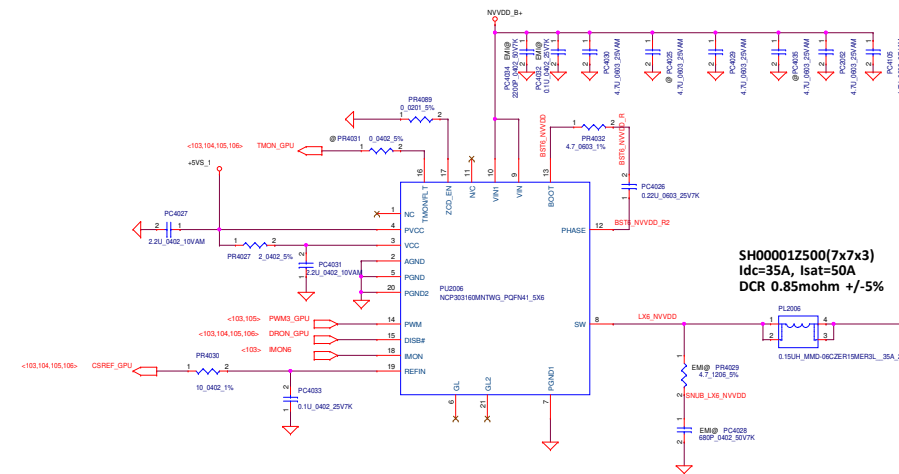
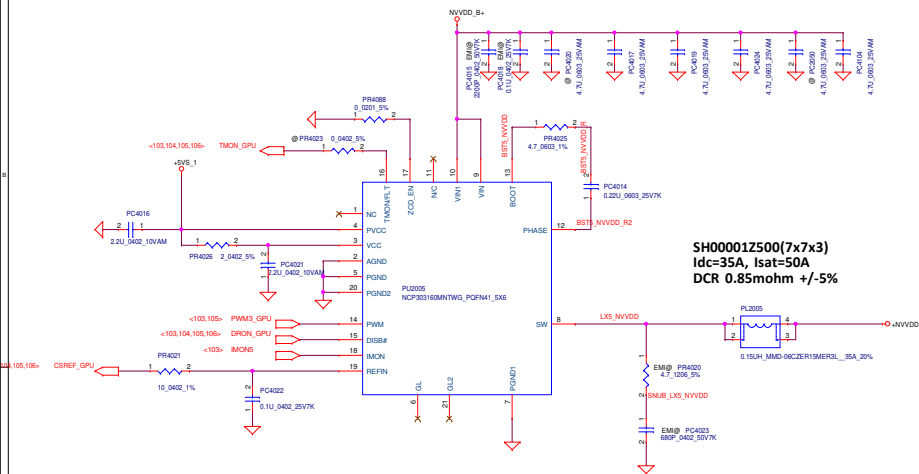
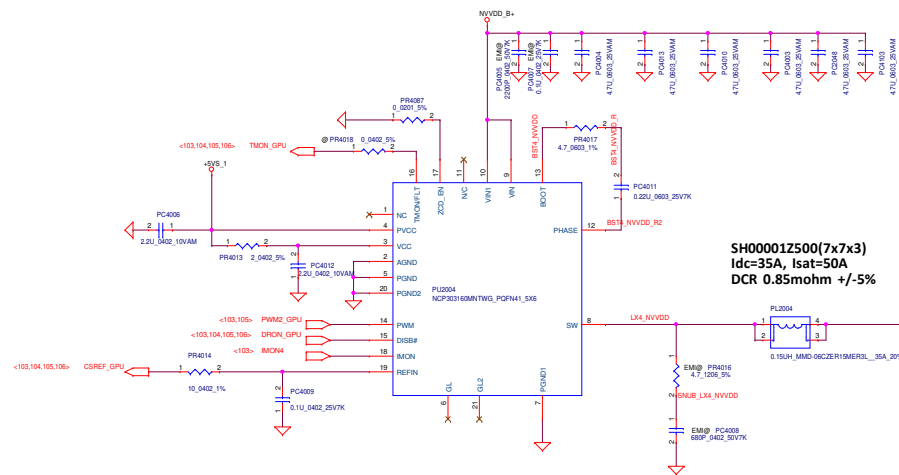
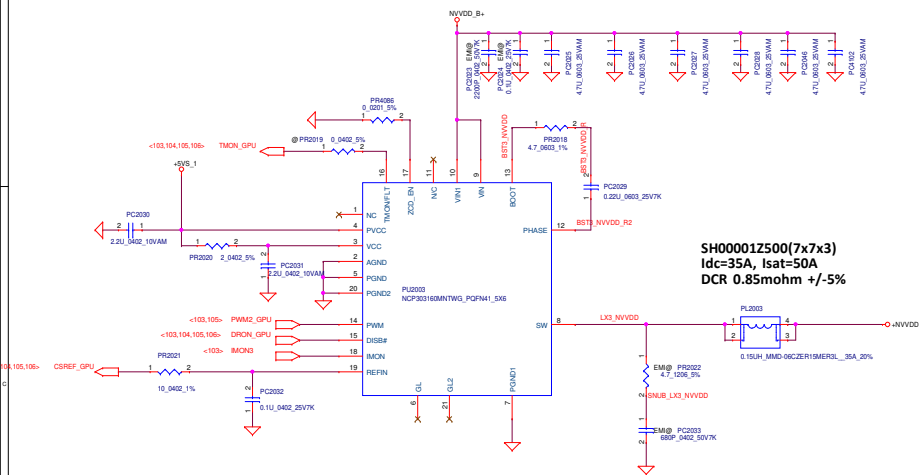
Config	
Vmin	0.3
Vmax	1.3
Vboot	0.75
R1	6.19K
R2	<30.37,58.64,85>
R3	<30.37,58.64,85>
R4	13.7K
R5	0.274
C	4.7n

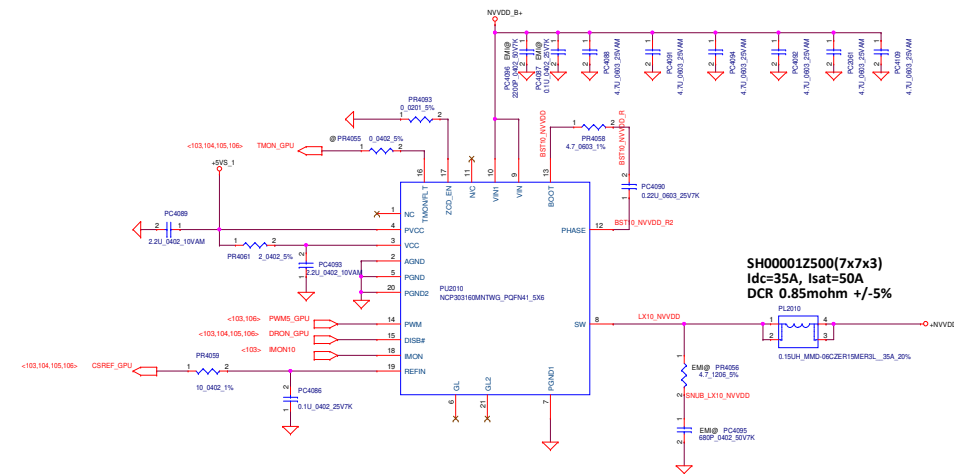
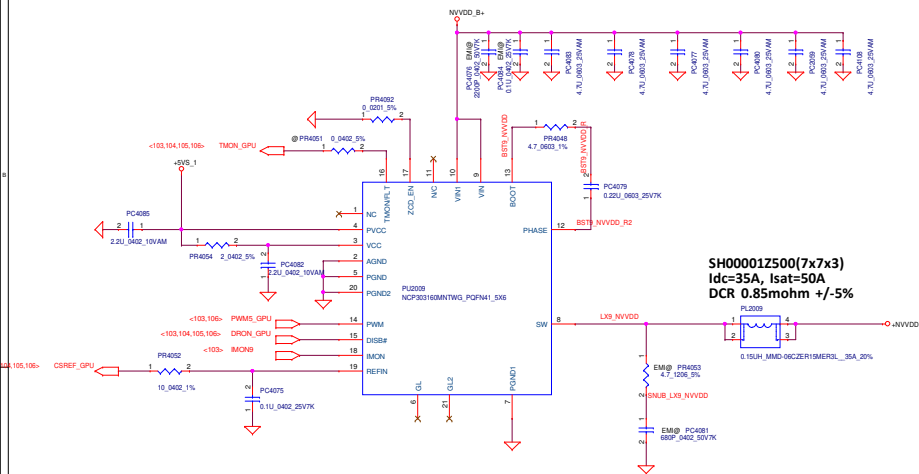
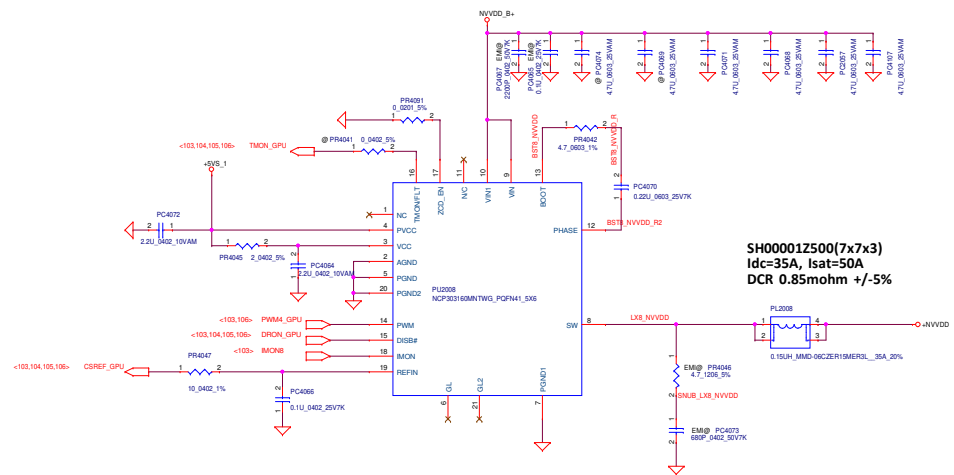
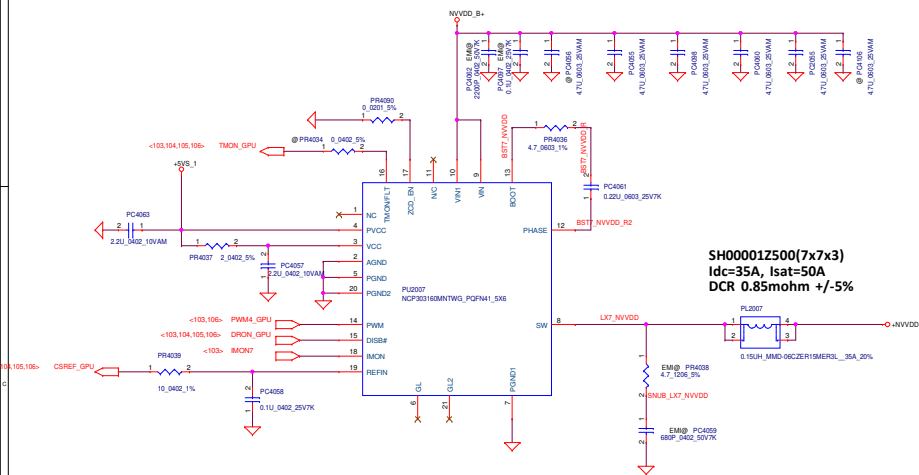
	Pull down R	
PWM1/PHTH4	NA	Function Disabled
PWM2/PHTH3	NA	Function Disabled
PWM3/PHTH2	NA	Function Disabled
PWM4/PHTH1	NA	Function Disabled
PWM5/LPC2	10K	CCM Mode
PWM6/LPC1	10K	CCM Mode
PWM7/I2C	26.1K	Address: 0x50
PWM8/SS	26.1K	0.6s

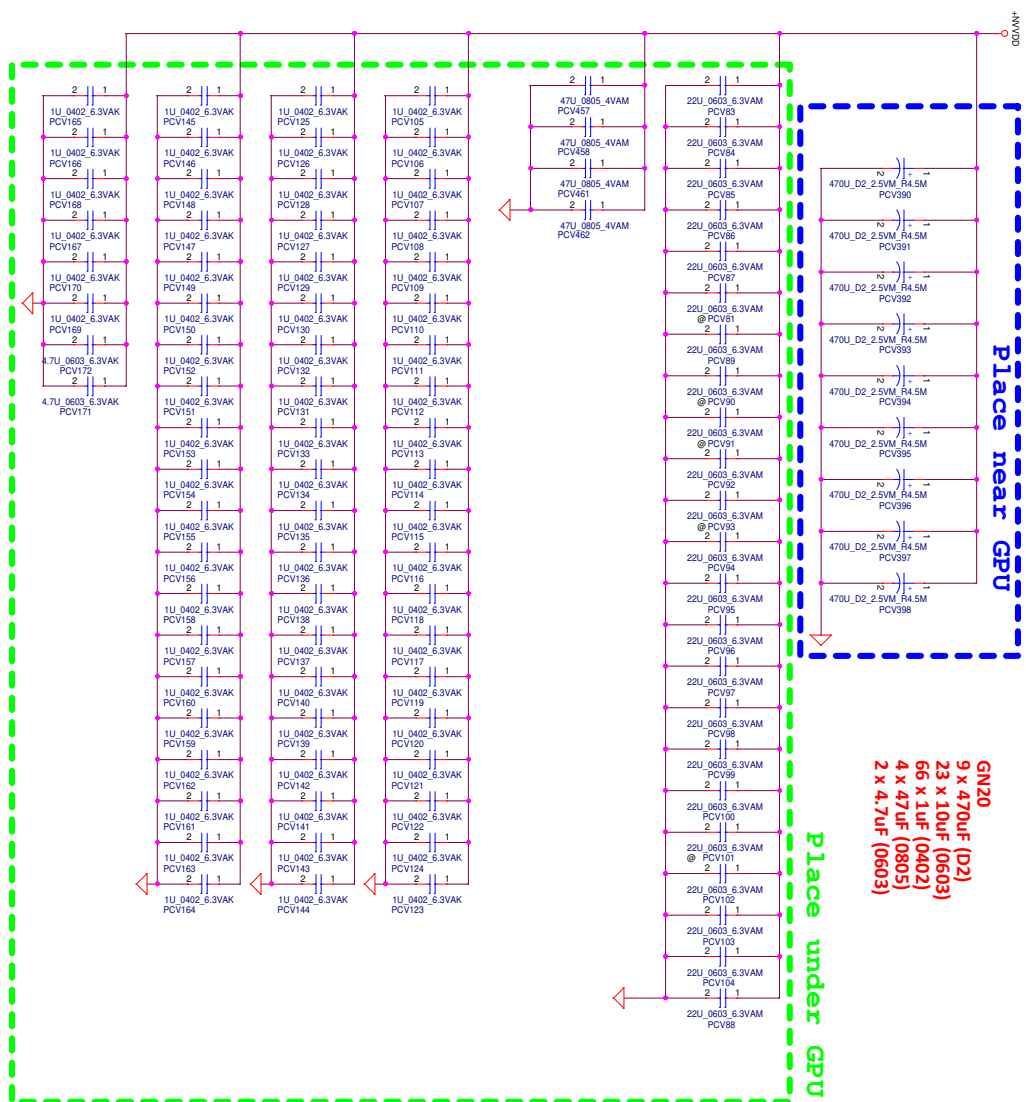
GPU	E5/E7-MAXP	E3-MAXP
EDP-P	297A	375A
BOM structure	150WON160@	115WON160@
PR1028	27.4K	23.7K
PR1029	45.3K	56.2K
PR1037	301K	274K



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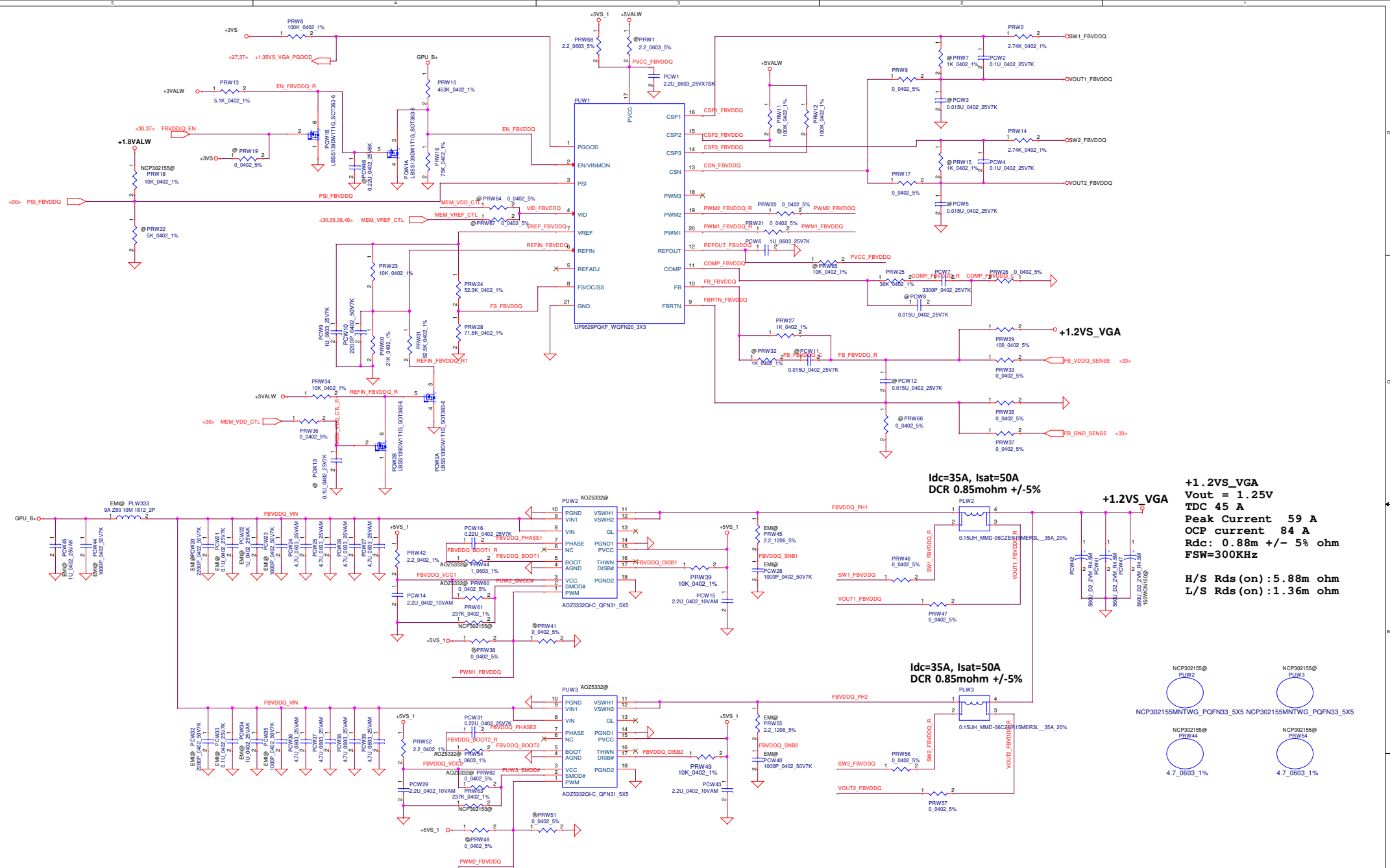


GN20
9 x 470uF (D2)
23 x 10uF (0603)
66 x 1uF (0402)
4 x 47uF (0805)
2 x 4.7uF (0603)

Place under GPU

Place near GPU

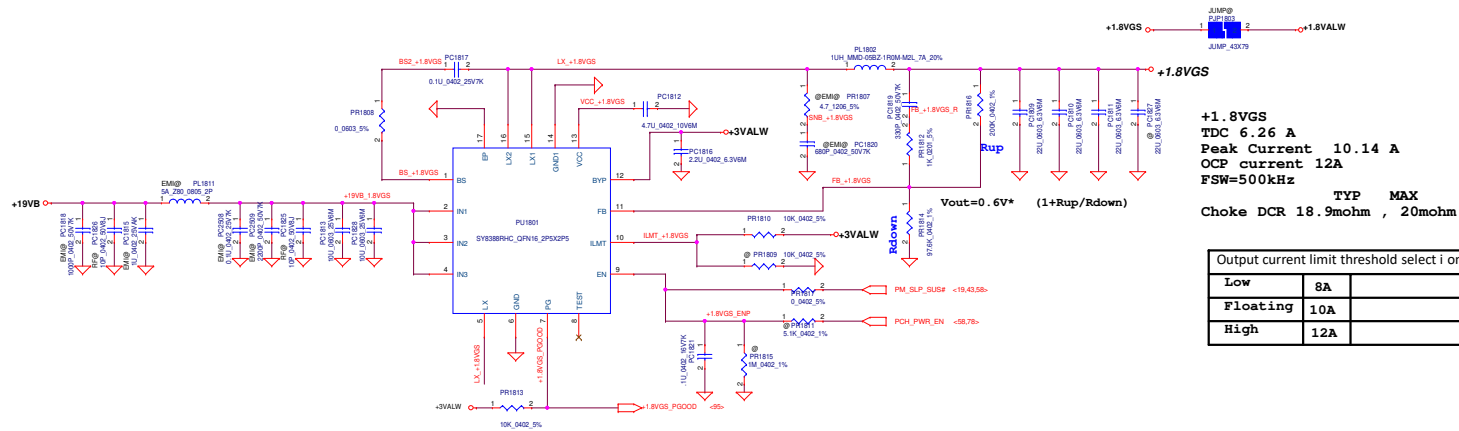
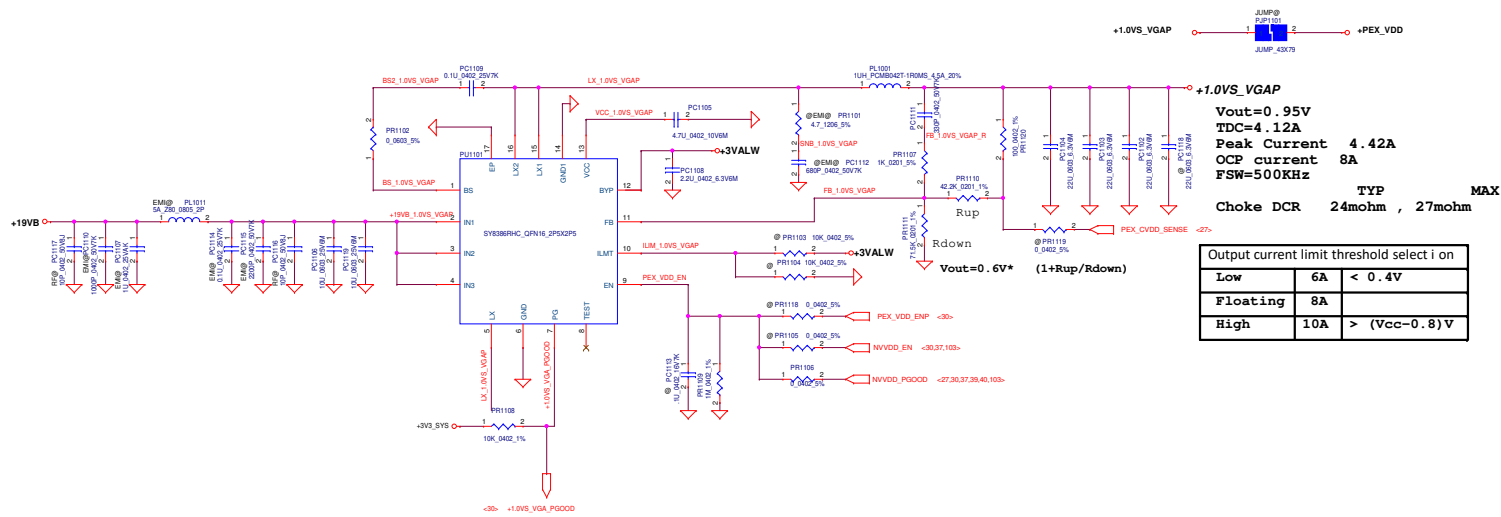
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Issued Date	2020/02/27	Declassified Date	2027/1/23/	Title	
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Date	Thursday, February 13, 2025			Sheet	107 of 121



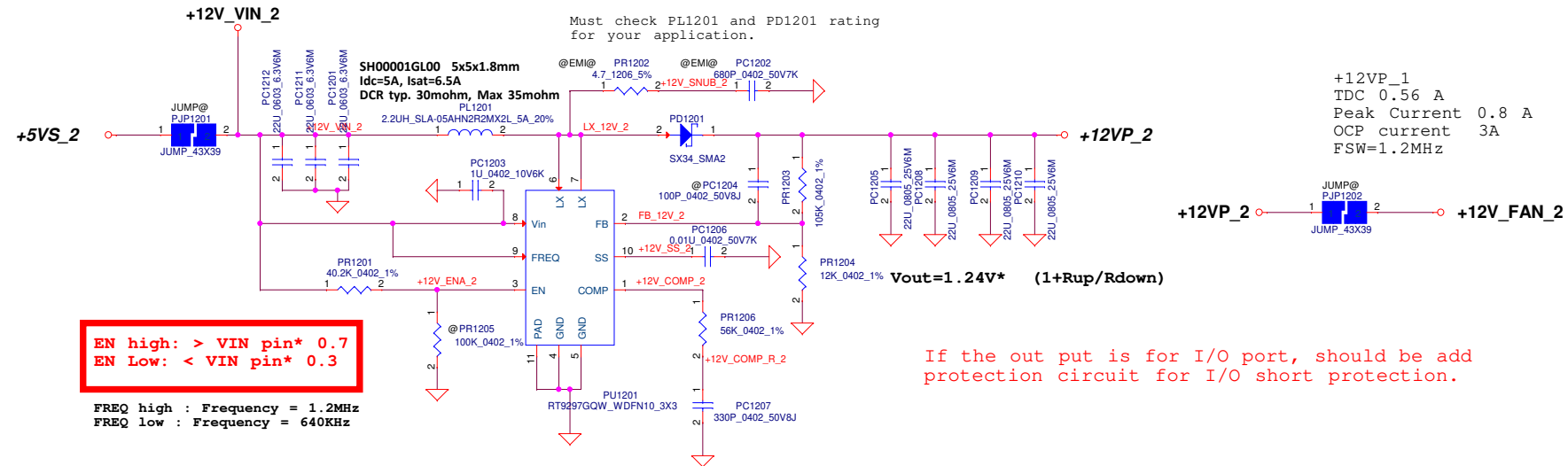
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Issued Date	2020/02/27	Deciphered Date	2021/12/31	PWR GPU VRAM	
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Date: Thursday, February 18, 2021				Sheet	108 of 121

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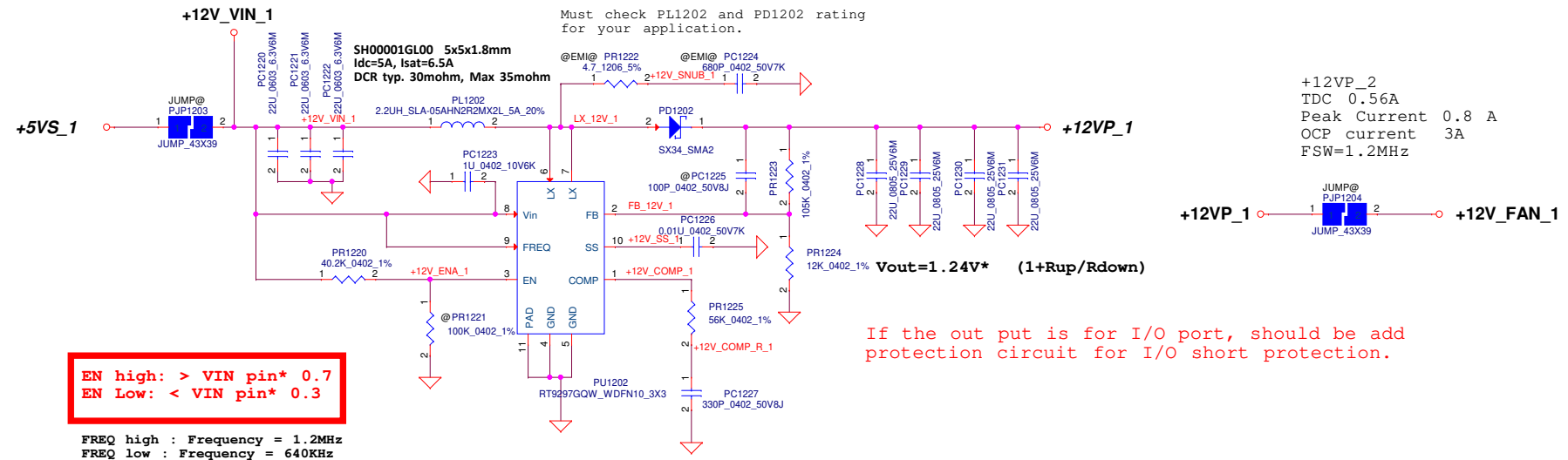
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Add a switch circuit to turn off the +12V_VIN if need.

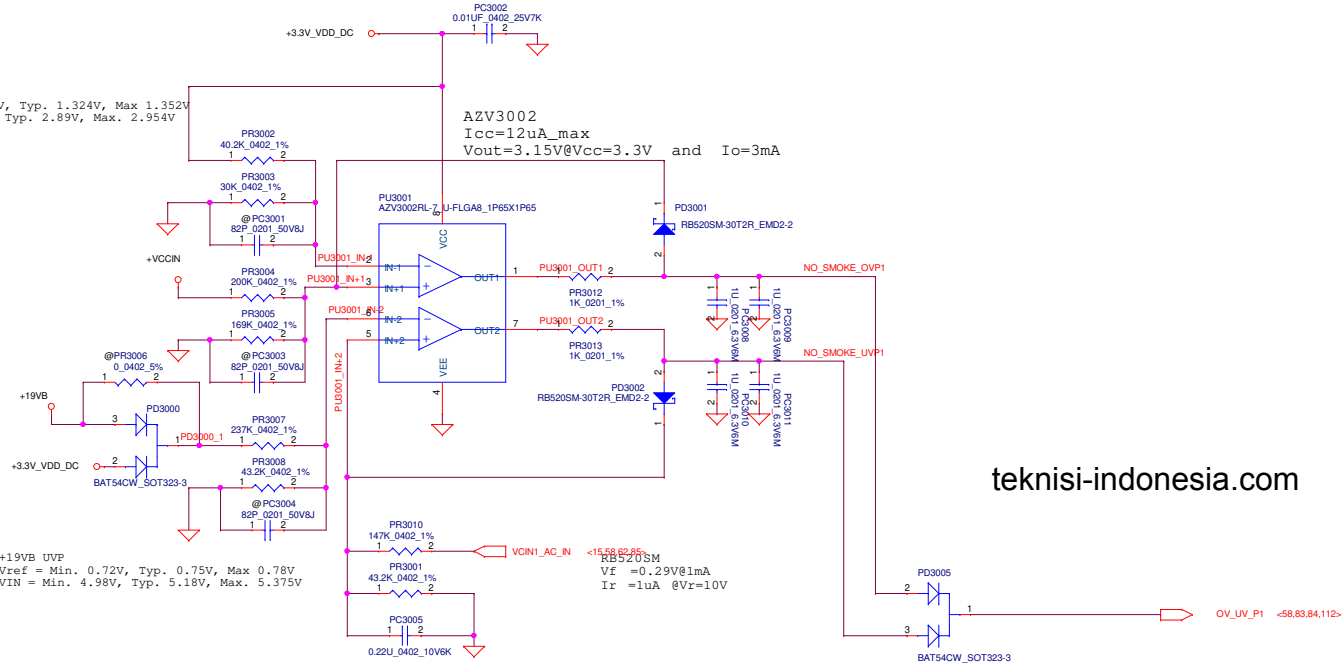


Add a switch circuit to turn off the +12V_VIN if need.



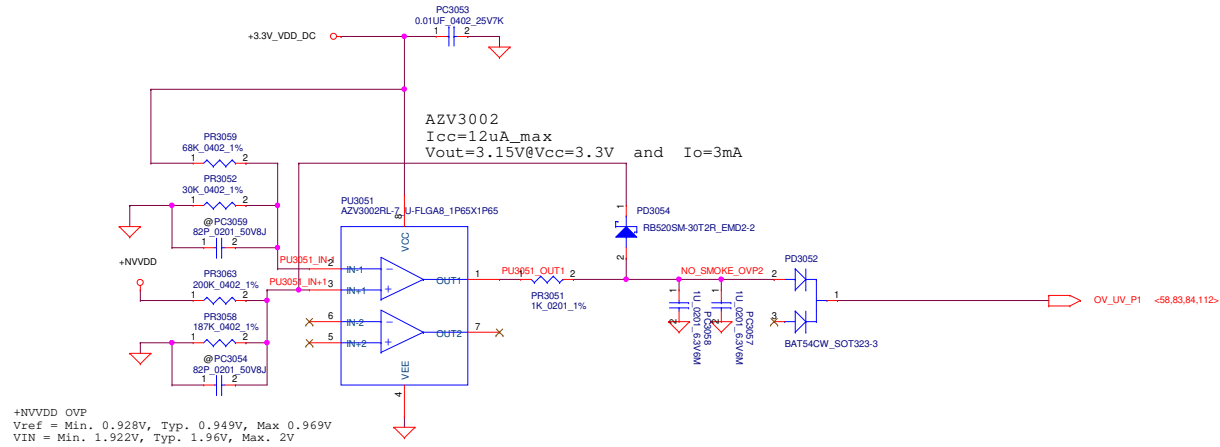
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Size		Document Number		Rev	
		LA-K472P		0.1	
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+VCCIN OVP
Vref = Min. 1.296V, Typ. 1.324V, Max 1.352V
VIN = Min. 2.83V, Typ. 2.89V, Max. 2.954V



teknisi-indonesia.com

+19VB UVP
Vref = Min. 0.72V, Typ. 0.75V, Max 0.78V
VIN = Min. 4.98V, Typ. 5.18V, Max. 5.375V



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	97	PWR-IMVP9-NCP81308	2020/10/13	PWR	Setting PSYS resistor meet system request	Change PRZ39 from SD034200280 (S RES 1/16W 20K +-1% 0402) to (S RES 1/16W 16.2K +-1%)	0.1
2	83	PWR_2 Type-C PD Selector	2020/10/13	PWR	For vendor request,add 4.7uf on output	Add PC914 and PC915 SE00001CJ00(4.7U_25V) on output pin	0.1
3	110	PWR_GPU_PEXVDD/1.8VGS	2020/10/13	PWR	Change pull high net of +1.8VGS_PGOOD for sequency	Change pull high net of +1.8VGS_PGOOD from +3VS to +3VALW	0.1
4	82	PWR_DCIN / BATT CONN / OTP	2020/10/13	PWR	Change one shot PROCHOT timing to link software	Change PR33 from SD034470280(47K) to SD034137380(137K) Change PR29 from SD034300380(300K) to SD034113380(113K) Change PR28 from SD034100380(100K) to SD034154380(154K)	0.1
5	83	PWR_2 Type-C PD Selector	2020/10/13	PWR	Change one shot PROCHOT timing to link software	Change PRS29,PRS33 from SD034470280(47K) to SD034137380(137K) Change PRS54,PRS31 from SD034300380(300K) to SD034100380(100K)	0.1
6	96	PWR_VCCIN_AUX DECOUPLING	2020/10/13	PWR	Reserve 330uF B2 for acoustic issue	Add PCC84 SGA00007Z00(S POLY C 330U 2.5V M B2 ESR9M PSG H1.9)	0.1
7	95	PWR_VCCIN_AUX-RT6543A	2020/10/13	PWR	For intel leakage voltage issue change from VNN_V1.05A_BYPASS_PWRGD to PG_VCCIN_AUX	Add PG_VCCIN_AUX link to VNN_V1.05A_BYPASS_PWRGD with 0 ohm	0.1
8	108	PWR_GPU_VRAM	2020/10/13	PWR	For Nvidia V04 spec, change FBVDD OCP	PRW24 change from SD034499280(49.9K) to SD034523280(52.3K) PRW28 change from SD034750280(75K) to SD034680280(68K)	0.1
9	82	PWR_DCIN / BATT CONN / OTP	2020/10/13	PWR	Modify prochot low level voltage	Removed PD7,PD8 Add PQ3214,PQ3215	0.1
10	83	PWR_2 Type-C PD Selector	2020/10/13	PWR	Modify prochot low level voltage	Removed PDS18,PDS19 Add PQS73,PQS74	0.1
11	108	PWR_GPU_VRAM	2020/10/13	PWR	Reduce Vds overshoot for snubber change by real measure	PRW44, PRW54 change from SD014000080(0) to SD014100B80(1) PRW45, PRW55 change from SD001470B80(4.7) to SD011220B80(2.2) PCW28, PCW40 change from SE074681K8(680P) to SE074102K80(1000P)	0.1
12	108	PWR_GPU_VRAM	2020/10/28	PWR	For vender recommend	PRW2,PRW4 change from SD000000UV00(3.6K) to SD034274180(2.74k)	0.1
13	97	PWR-IMVP9-NCP81305	2020/10/28	PWR	Vender recommend by VRTT	PRZ11 change to SD034127380(127K) PRZ6 change to SD034261280(26.1K) PRZ21,PRZ22,PRZ23,PRZ24,PRZ96,PRZ97 change to SD0000004J80(4.42K) PCZ8 change to SE071121J80(120P)	0.1
14	85	PWR_CHARGER-ISL9241	2020/10/28	PWR	EMI request snubber RC stuff	PRB17,PRB18,PCB30,PCB69 stuff	0.1
15	85	PWR_CHARGER-ISL9241	2020/10/28	PWR	For DIDD A04 spec	PCB21 change to X6S(SE00001CJ00)	0.1
16	95	PWR_VCCIN_AUX-RT6543A	2020/10/28	PWR	For DIDD A04 spec	PCG1,PCI1 change to X7R(SE00000W210)	0.1
17	87	+3.3VALWP/+5VALWP	2020/10/30	PWR	+3VLP series 0ohm	Add PR336_SD013000080	0.1

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	91	PWR_BYPASS (APW8743C)	2020/10/30	PWR	EMI request	PC1515,PC1516 change to pop PR1505,PR1506 change to pop	0.1
2	83	Type-C PD Selector	2020/10/30	PWR	shortage	PQS73,PQS74 change from SB000016L00 to SB00000T000	0.1
3	84	DCIN/TypeC	2020/10/30	PWR	shortage	PQ11 change from SB00001FI00 to SB000011K00 PQ57 change from SB00001RK00 to SB000013X00	0.1
4	85	CHARGER-ISL9241	2020/10/30	PWR	shortage	PQB14 change from SB00001PI00 to SB000011K00 PQB13 change from SB00001RK00 to SB000013X00	0.1
5	104	GPU_CORE_SW1&2	2020/10/30	PWR	EMI request	Removed PJPV01,PJPV02 Add PL1901~PL1903_SM01000U600	0.1
6	108	GPU_VRAM	2020/12/28	PWR	PUW1 PVCC pin change connect to +5VS	Add PRW68 SD013220B80 PRW1 bom structure change to @	0.2
7	108	GPU_VRAM	2020/12/28	PWR	+1.2VS_VGA OCP adjust	PWR28 change from SD034680280 to SD034715280	0.2
8	108	GPU_VRAM	2020/12/28	PWR	For vender recommend	PCW46 bom structure change to @	0.2
9	84	DCIN/TypeC	2021/01/13	PWR	EMI request	PC1,PC3 change from SE071101J80 to SE000012Q80	0.2
10	85	CHARGER-ISL9241	2021/01/13	PWR	EMI request	Add SE00000W210*10,PCB98~PCB107(EMI@)	0.2
11	107	GPU_ DECOUPLING	2021/01/13	PWR	For VRAM ripple, reserved placement to EE add MLCC	Removed PCV459,PCV460,PCV463	0.2
12	108	GPU_VRAM	2021/01/20	PWR	For VRAM ripple	Add PCW47_SGA0000D600 PLW2,PLW3 change from SH00001FK00 to SH00001Z500	0.2
13	85	CHARGER-ISL9241	2021/01/20	PWR	130W TypeC smokeless issue	PRB6 change from SD014330B80 to SD014100B80	0.2
14	84	DCIN/TypeC_PW	2021/01/27	PWR	shortage	PQ802 change from SB00001SS00 to SB00001ST00	0.2
15	95	VCCIN_AUX-RT6543A_PW	2021/01/27	PWR	For DIDT	PCG5,PCG6,PCH,PC6 change from SE000000K80 to SE000000WV00	0.2
16	104-107	GPU_CORE_SW1&2_PW	2021/01/27	PWR	EMI issue	bom structure change to pop PC2025, PC4004, PC2048, PC4102, PC4094, PC4083, PC4109, PC4080, PCV98, PCV85, PCV104, PCV84	0.2

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